查询MB89490_03供应商

FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12560-1E

*8-bit Proprietary Microcontroller*

**CMOS**

# F²MC-8L MB89490 Series

# MB89498/F499/PV490

## ■ DESCRIPTION

The MB89490 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit single-chip microcontrollers.

In addition to a compact instruction set, the general-purpose, single-chip microcontroller contains a variety of peripheral functions such as 21-bit timebase timer, watch prescaler, PWM timer, 8/16-bit timer/counter, remote receiver circuit, LCD controller/driver, external interrupt 0 (edge) , external interrupt 1 (level) , 10-bit A/D converter, UART/SIO, SIO, I²C and watchdog timer reset.

The MB89490 series is designed suitable for compact disc/radio receiver controller as well as in a wide range of applications for consumer product.

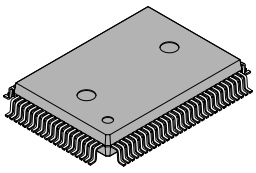
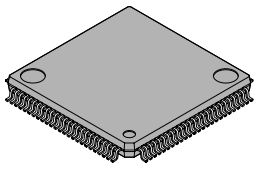
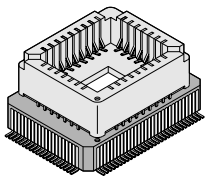
* : “F²MC”, an abbreviation for FUJITSU Flexible Microcontroller, is a registered trademark of FUJITSU Ltd.

## ■ FEATURES

- Package
  QFP, LQFP package for MB89F499, MB89498
  MQFP package for MB89PV490

*(Continued)*

## ■ PACKAGES

| 100-pin Plastic QFP | 100-pin Plastic LQFP | 100-pin Ceramic MQFP |
|---|---|---|
|  |  |  |
| (FTP-100P-M06) | (FTP-100P-M05) | (MQP-100C-P01) |

FUJITSU

*(Continued)*

- High speed operating capability at low voltage
- Minimum execution time : 0.32 μs/12.5 MHz
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Branch instructions by test bit
  - Bit manipulation instructions, etc.

- PLL circuit for sub-clock
  - Embedded for PLL clock multiplication circuit for sub-clock
  - Operating clock (PLL for sub-clock) can be selected from no multiplication or 4 times of the sub-clock oscillation frequency.
- 6 timers
  PWM timer × 2
  8/16-bit timer/counter × 2
  21-bit timebase timer
  Watch prescaler
- External interrupt
  Edge detection (selectable edge) : 8 channels
  Low level interrupt (wake-up function) : 8 channels
- 10-bit A/D converter (8 channels)
  10-bit successive approximation type
- UART/SIO
  Synchronous/asynchronous data transfer capability
- SIO
  Switching of synchronous data transfer capability
- LCD controller/driver
  Max 32 segments output × 4 commons
- I²C interface circuit
- Remote receiver circuit
- Low-power consumption mode
  Stop mode (oscillation stops so as to minimize the current consumption.)
  Sleep mode (CPU stops so as to reduce the current consumption to approx. 1/3 of normal.)
  Watch mode (operation except the watch prescaler stops so as to reduce the power comsumption to an extremely low level.)
  Sub-clock mode
- Watchdog timer reset
- I/O ports : Max 66 channels

## ■ PRODUCT LINEUP

| Parameter \ Part number | MB89498 | MB89F499 | MB89PV490 |
|---|---|---|---|
| Classification | Mass production products (mask ROM product) | FLASH | Piggy-back (For evaluation or development) |
| ROM size | 48 K × 8-bit (internal ROM) | 60 K × 8-bit (internal FLASH) | 60 K × 8-bit (external ROM) *1 |
| RAM size | 2 K × 8-bit | 2 K × 8-bit | 2 K × 8-bit |
| CPU functions | Number of instructions : 136<br>Instruction bit length : 8-bit<br>Instruction length : 1 to 3 bytes<br>Data bit length : 1-bit, 8-bit, 16-bit<br>Minimum instruction execution time : 0.32 µs/12.5 MHz<br>Minimum interrupt processing time : 2.88 µs/12.5 MHz | | |
| Ports | General-purpose I/O ports (CMOS) : 56 pins<br>Input ports (CMOS) : 2 pins<br>N-channel open drain I/O ports : 8 pins<br>Total : 66 pins | | |
| 21-bit timebase timer | Interrupt generation cycle (0.66 ms, 2.6 ms, 21.0 ms, 335.5 ms) at 12.5 MHz | | |
| Watchdog timer | Reset generation cycle (167.8 ms to 335.5 ms) at 12.5 MHz | | |
| PWM timer 0, 1 | 8-bit reload timer operation (supports square wave output and operating clock period : 1 $t_{inst}$, 8 $t_{inst}$, 16 $t_{inst}$, 64 $t_{inst}$ )<br>8-bit accuracy PWM operation | | |
| 8/16-bit timer/counter 00, 01 | Can be operated either as a 2-channel 8-bit timer/counter (timer 00 and timer 01, each with its own independent operating clock) , or as one 16-bit timer/counter.<br>In timer 00 or 16-bit timer/counter operation, event counter operation by external clock input and square wave output capability | | |
| 8/16-bit timer/counter 10, 11 | Can be operated either as a 2-channel 8-bit timer/counter (timer 10 and timer 11, each with its own independent operating clock) , or as one 16-bit timer/counter.<br>In timer 10-bit or 16-bit timer/counter operation, event counter operation by external clock input and square wave output capability | | |
| External interrupt 0 (edge) | 8 independent channels (selectable edge, interrupt vector, request flag) | | |
| External interrupt 1 (level) | 8 channels (low level interrupt) | | |
| A/D converter | 10-bit accuracy × 8 channels<br>A/D conversion function (conversion time : 30 $t_{inst}$ )<br>Supports repeated activation by internal clock | | |
| LCD controller/driver | Common output : 4 (Max)<br>Segment output : 32 (Max)<br>LCD driving power (bias) pins : 3<br>LCD display RAM size : 32 × 4 bits | | |

*(Continued)*

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| Part number / Parameter | MB89498 | MB89F499 | MB89PV490 |
|---|---|---|---|
| UART/SIO | Synchronous/asynchronous data transfer capability<br>(Max baud rate : 97.656 Kbps at 12.5 MHz)<br>(7-bit and 8-bit with parity bit; 8-bit and 9-bit without parity bit) | | |
| SIO | 8-bit serial I/O with LSB first/MSB first selectability<br>1 clock selectable from 4 operation clock (1 external shift clock and 3 internal shift clock : 0.64 µs, 2.56 µs, 10.24 µs at 12.5 MHz) | | |
| $I^2C$*2 | 1 channel<br>(Use a 2-wire protocol to communicate with other device) | | |
| Remote receiver circuit | Selectable maximum noise width removal<br>Reversible input polarity | | |
| Standby mode | Sleep mode, stop mode, watch mode and sub-clock mode | | |
| Process | CMOS | | |
| Operating voltage | 2.2 V to 3.6 V | 2.7 V to 3.6 V | 2.7 V to 3.6 V |

*1 : Use MBM27C512 as the external ROM.

*2 : $I^2C$ is complied to Philips $I^2C$ specification.

## ■ PACKAGE AND CORRESPONDING PRODUCTS

| Parameter \ Part number | MB89498 | MB89F499 | MB89PV490 |
|---|---|---|---|
| FPT-100P-M06 | O | O | × |
| FPT-100P-M05 | O | O | × |
| MQP-100C-P01 | × | × | O |

O : Availabe
× : Not available

## ■ DIFFERENCES AMONG PRODUCTS

### 1. Memory Size

Before evaluating using the piggy-back product, verify its differences from the product that will be actually used. Take particular care on the following point : The stack area is set at the upper limit of the RAM.

### 2. Current Consumption

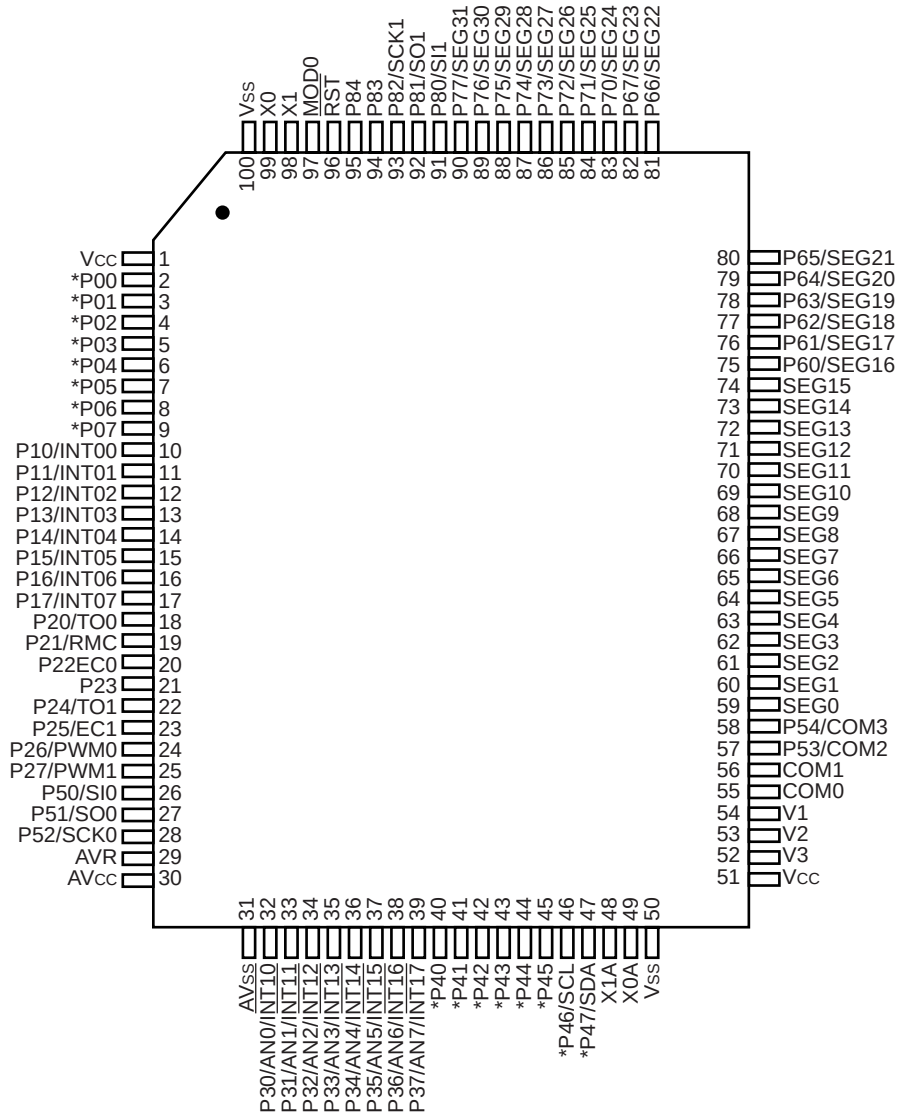
- For the MB89PV490, add the current consumed by the EPROM mounted in the piggy-back socket.
- When operating at low speed, the current consumed by the FLASH product is greater than that for the mask ROM product. However, the current consumption is roughly the same in sleep and stop mode.
- For more information, see “■ ELECTRICAL CHARACTERISTICS.”

### 3. Oscillation Stabilization Wait Time after Power-on Reset

- For MB89PV490 and MB89F499, the power-on stabilization wait time cannot be selected after power-on reset.
- For MB89498, the power-on stabilization wait time can be selected after power-on reset.
- For more information, please refer to “■ MASK OPTIONS”.

## ■ PIN ASSIGNMENTS

(TOP VIEW)

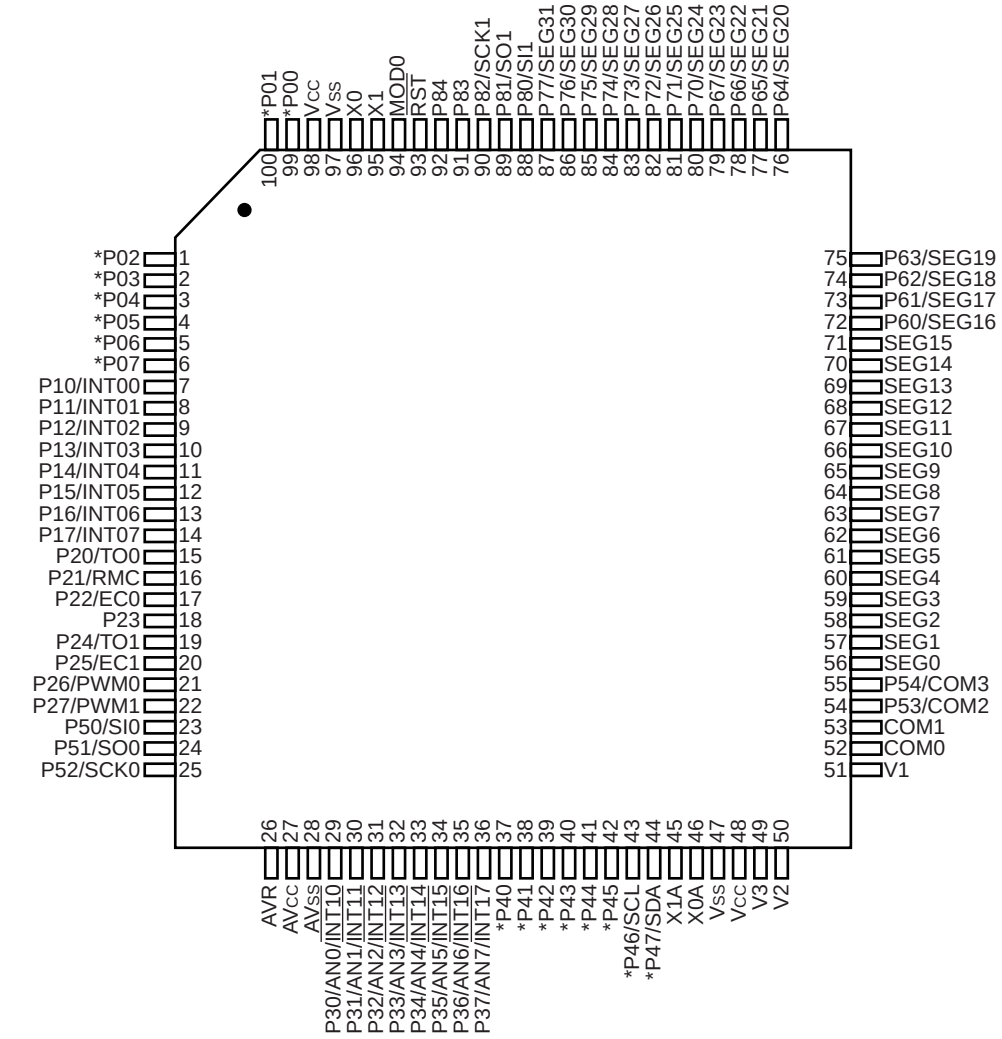



(FPT-100P-M06)

* : High current pins

*(Continued)*

(TOP VIEW)



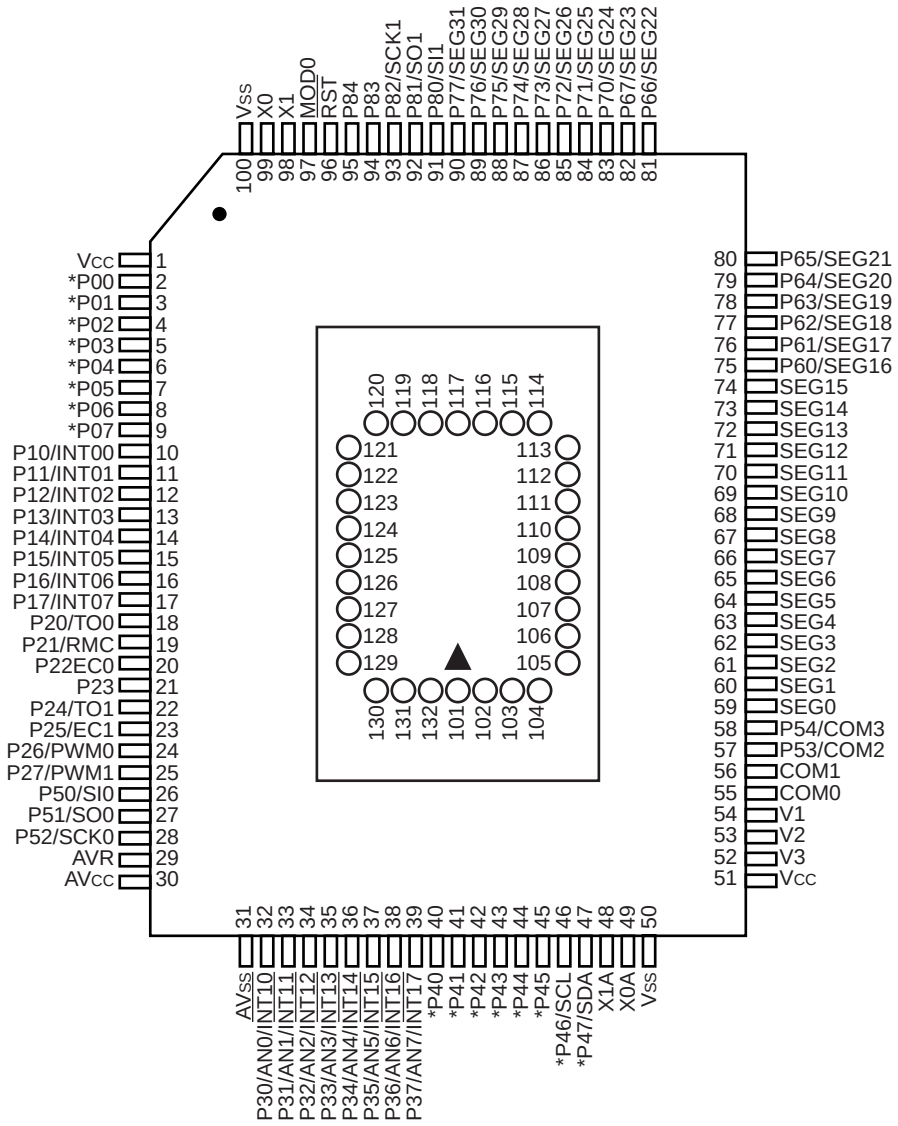

(FPT-100P-M05)

* : High current pins

*(Continued)*

*(Continued)*

(TOP VIEW)




* : High current pins

(MQP-100C-P01)

Pin assignment on package top (MB89PV490 only)

| Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name | Pin no. | Pin name |
|---|---|---|---|---|---|---|---|---|---|
| 101 | N.C. | 108 | A3 | 115 | O3 | 122 | O8 | 129 | A8 |
| 102 | A15 | 109 | A2 | 116 | $V_{SS}$ | 123 | $\overline{CE}$ | 130 | A13 |
| 103 | A12 | 110 | A1 | 117 | N.C. | 124 | A10 | 131 | A14 |
| 104 | A7 | 111 | A0 | 118 | O4 | 125 | $\overline{OE}$ | 132 | $V_{CC}$ |
| 105 | A6 | 112 | N.C. | 119 | O5 | 126 | N.C. | | |
| 106 | A5 | 113 | O1 | 120 | O6 | 127 | A11 | | |
| 107 | A4 | 114 | O2 | 121 | O7 | 128 | A9 | | |

N.C. : As connected internally, do not use.

## ■ PIN DESCRIPTION

| Pin number | | Pin name | I/O circuit type | Function |
|---|---|---|---|---|
| MQFP*1/ QFP*2 | LQFP*3 | | | |
| 99 | 96 | X0 | A | Connection pins for a crystal or other oscillator circuit.<br>An external clock can be connected to X0. In this case, leave X1 open. |
| 98 | 95 | X1 | | |
| 49 | 46 | X0A | A | Connection pins for a crystal or other oscillator circuit.<br>An external clock can be connected to X0A. In this case, leave X1A open. |
| 48 | 45 | X1A | | |
| 97 | 94 | MOD0 | B | Input pin for setting the memory access mode.<br>Connect directly to $V_{SS}$. |
| 95, 94 | 92, 91 | P84, P83 | J | General-purpose CMOS input port. |
| 96 | 93 | $\overline{RST}$ | C | Reset I/O pin. The pin is an N-ch open-drain type with pull-up resistor and hysteresis input. The pin outputs an “L” level when an internal reset request is present. Inputting an “L” level initializes internal circuits. |
| 2 to 9 | 99 to 6 | P00 to P07 | D | General-purpose CMOS I/O port. |
| 10 to 17 | 7 to 14 | P10/INT00 to P17/INT07 | E | General-purpose CMOS I/O port.<br>The pin is shared with external interrupt 0 input. |
| 18 | 15 | P20/TO0 | F | General-purpose CMOS I/O port.<br>The pin is shared with 8/16-bit timer/counter 00 and 01 output. |
| 19 | 16 | P21/RMC | E | General-purpose CMOS I/O port.<br>The pin is shared with remote receiver input. |
| 20 | 17 | P22/EC0 | E | General-purpose CMOS I/O port.<br>The pin is shared with 8/16-bit timer/counter 00 and 01 input. |
| 21 | 18 | P23 | F | General-purpose CMOS I/O port. |
| 22 | 19 | P24/TO1 | F | General-purpose CMOS I/O port.<br>The pin is shared with 8/16-bit timer/counter 10 and 11 output. |
| 23 | 20 | P25/EC1 | E | General-purpose CMOS I/O port.<br>The pin is shared with 8/16-bit timer/counter 10 and 11 input. |
| 24 | 21 | P26/PWM0 | F | General-purpose CMOS I/O port.<br>The pin is shared with PWM0 output. |
| 25 | 22 | P27/PWM1 | F | General-purpose CMOS I/O port.<br>The pin is shared with PWM1 output. |
| 32 to 39 | 29 to 36 | P30/AN0/$\overline{INT10}$ to P37/AN7/$\overline{INT17}$ | G | General-purpose CMOS I/O port.<br>The pin is shared with external interrupt 1 input and A/D converter input. |
| 40 to 45 | 37 to 42 | P40 to P45 | H | General-purpose N-ch open-drain I/O port. |
| 46 | 43 | P46/SCL | H | General-purpose N-ch open-drain I/O port.<br>The pin is shared with $I^2C$ clock I/O. |

*(Continued)*

*(Continued)*

| Pin number | | Pin name | I/O circuit type | Function |
|---|---|---|---|---|
| MQFP*1/ QFP*2 | LQFP*3 | | | |
| 47 | 44 | P47/SDA | H | General-purpose N-ch open-drain I/O port.<br>The pin is shared with $I^2C$ data I/O. |
| 26 | 23 | P50/SI0 | E | General-purpose CMOS I/O port.<br>The pin is shared with SIO data input. |
| 27 | 24 | P51/SO0 | F | General-purpose CMOS I/O port.<br>The pin is shared with SIO data output. |
| 28 | 25 | P52/SCK0 | E | General-purpose CMOS I/O port.<br>The pin is shared with SIO clock I/O. |
| 57 | 54 | P53/COM2 | F/I | General-purpose CMOS I/O port.<br>The pin is shared with the LCD common output. |
| 58 | 55 | P54/COM3 | F/I | General-purpose CMOS I/O port.<br>The pin is shared with the LCD common output. |
| 75 to 82 | 72 to 79 | P60/SEG16 to P67/SEG23 | F/I | General-purpose CMOS I/O port.<br>The pin is shared with LCD segment output. |
| 83 to 90 | 80 to 87 | P70/SEG24 to P77/SEG31 | F/I | General-purpose CMOS I/O port.<br>The pin is shared with LCD segment output. |
| 91 | 88 | P80/SI1 | E | General-purpose CMOS I/O port.<br>The pin is shared with UART/SIO data input. |
| 92 | 89 | P81/SO1 | F | General-purpose CMOS I/O port.<br>The pin is shared with UART/SIO data output. |
| 93 | 90 | P82/SCK1 | E | General-purpose CMOS I/O port.<br>The pin is shared with UART/SIO clock I/O. |
| 59 to 74 | 56 to 71 | SEG0 to SEG15 | I | LCD segment output-only pin. |
| 55, 56 | 52, 53 | COM0, COM1 | I | LCD common output-only pin. |
| 54, 53, 52 | 51, 50, 49 | V1 to V3 | — | LCD driving power supply pin. |
| 1, 51 | 98, 48 | $V_{CC}$ | — | Power supply pin. |
| 50, 100 | 47, 97 | $V_{SS}$ | — | Power supply pin (GND) . |
| 30 | 27 | $AV_{CC}$ | — | A/D converter power supply pin. |
| 29 | 26 | AVR | — | A/D converter reference voltage input pin. |
| 31 | 28 | $AV_{SS}$ | — | A/D converter power supply pin.<br>Use at the same voltage level as $V_{SS}$. |

*1 : MQP-100C-P01

*2 : FPT-100P-M06

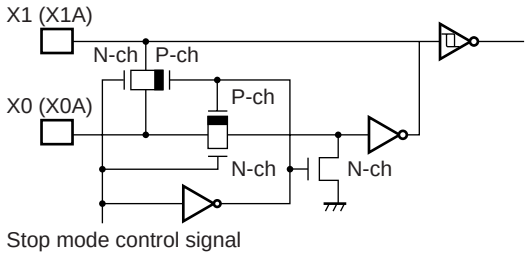
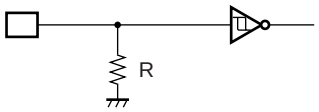
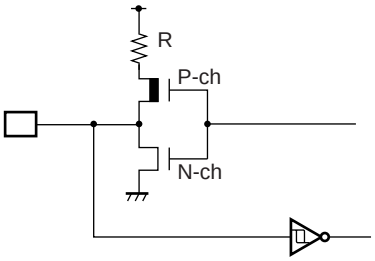
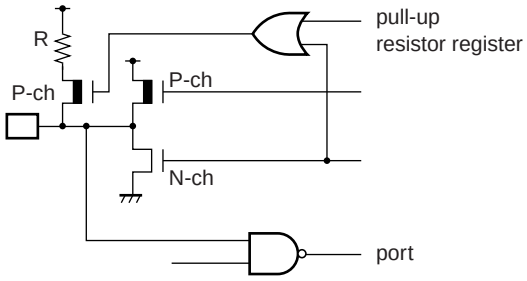
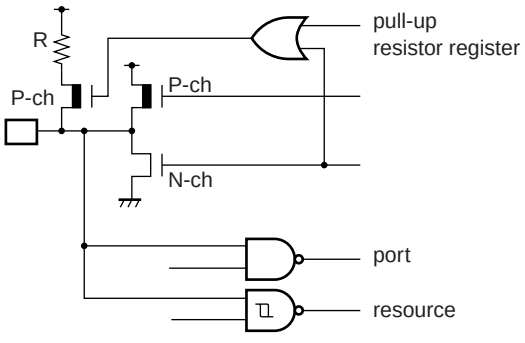
*3 : FPT-100P-M05

- **External EPROM Socket (MB89PV490 only)**

| Pin number MQFP* | Pin name | I/O | Function |
|---|---|---|---|
| 102<br>131<br>130<br>103<br>127<br>124<br>128<br>129<br>104<br>105<br>106<br>107<br>108<br>109<br>110<br>111 | A15<br>A14<br>A13<br>A12<br>A11<br>A10<br>A9<br>A8<br>A7<br>A6<br>A5<br>A4<br>A3<br>A2<br>A1<br>A0 | O | Address output pins. |
| 122<br>121<br>120<br>119<br>118<br>115<br>114<br>113 | O8<br>O7<br>O6<br>O5<br>O4<br>O3<br>O2<br>O1 | I | Data input pins. |
| 101<br>112<br>117<br>126 | N.C. | — | Internally connected pins. Always leave open. |
| 116 | $V_{SS}$ | O | Power supply pin (GND) . |
| 123 | $\overline{CE}$ | O | Chip enable pin for the EPROM. Outputs “H” in standby mode. |
| 125 | $\overline{OE}$ | O | Output enable pin for the EPROM. Always outputs “L”. |
| 132 | $V_{CC}$ | O | Power supply pin for the EPROM. |

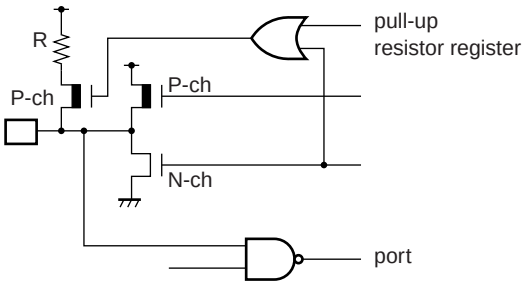
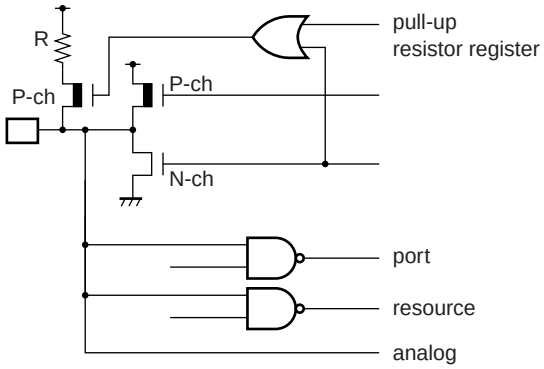
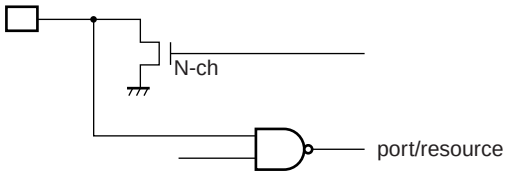
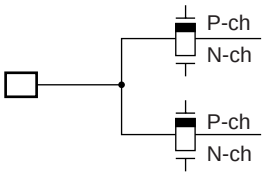
* : MQP-100C-P01

## ■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|---|---|---|
| A |  | • Main/Sub-clock circuit |
| B |  | • Hysteresis input<br>(CMOS input in MB89F499)<br>• The pull-down resistor<br>(not available in MB89F499)<br>Approx. 50 kΩ |
| C |  | • The pull-up resistor (P-channel)<br>Approx. 50 kΩ<br>• Hysteresis input |
| D |  | • CMOS output<br>• $I_{OH}$ = − 4 mA, $I_{OL}$ = 12 mA<br>• CMOS input<br>• Selectable pull-up resistor<br>Approx. 50 kΩ |
| E |  | • CMOS output<br>• $I_{OH}$ = − 2 mA, $I_{OL}$ = 4 mA<br>• CMOS port input<br>• Hysteresis resource input<br>• Selectable pull-up resistor<br>Approx. 50 kΩ |

*(Continued)*

*(Continued)*

| Type | Circuit | Remarks |
|---|---|---|
| F |  | • CMOS output<br>• $I_{OH}$ = − 2 mA, $I_{OL}$ = 4 mA<br>• CMOS input<br>• Selectable pull-up resistor<br>Approx. 50 kΩ |
| G |  | • CMOS output<br>• $I_{OH}$ = − 2 mA, $I_{OL}$ = 4 mA<br>• CMOS port input<br>• $V_{IH}$ = 0.85 $V_{CC}$, $V_{IL}$ = 0.5 $V_{CC}$ resource input<br>• Analog input<br>• Selectable pull-up resistor<br>Approx. 50 kΩ |
| H |  | • N-ch open-drain output<br>• $I_{OL}$ = 15 mA<br>• CMOS port input<br>• CMOS resource input<br>• 5 V tolerance |
| I |  | • LCD segment output |
| J | | • CMOS input |

## ■ HANDLING DEVICES

### 1. Preventing Latch-up

Latch-up may occur on CMOS IC if voltage higher than $V_{CC}$ or lower than $V_{SS}$ is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in “■ ELECTRICAL CHARACTERISTICS” is applied between $V_{CC}$ and $V_{SS}$.

When latch-up occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the maximum ratings.

Also, take care to prevent the analog power supply ($AV_{CC}$ and AVR) and analog input from exceeding the digital power supply ($V_{CC}$) when the analog system power supply is turned on and off.

### 2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

### 3. Treatment of Power Supply Pins on Microcontrollers with A/D

Connect to be $AV_{CC} = V_{CC}$ and $AV_{SS} = AVR = V_{SS}$ even if the A/D is not in use.

### 4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

### 5. Power Supply Voltage Stabilization

Although $V_{CC}$ power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. As stabilization guidelines, it is recommended to control voltage fluctuation so that $V_{CC}$ ripple fluctuations (P-P value) will be less than 10% of the standard $V_{CC}$ value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

### 6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset and wake-up from stop mode.

### 7. Treatment of Unused dedicated LCD pins

When dedicated LCD pins are not in use, keep them open.

## ■ PROGRAMMING AND ERASING FLASH MEMORY ON THE MB89F499

### 1. Flash Memory

The flash memory is located between $1000_H$ and $FFFF_H$ in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mask ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the internal CPU, providing an efficient method of updating program and data.

### 2. Flash Memory Features

- 60K bytes × 8-bit configuration (16 K + 8 K + 8 K + 28 K sectors)
- Automatic algorithm (Embedded algorithm* : Equivalent to MBM29LV200)
- Includes an erase pause and erase restart function
- Data polling and toggle bit for detection of program/erase completion
- Detection of program/erase completion via CPU interrupt
- Compatible with JEDEC-standard commands
- Sector Protection (sectors can be combined in any combination)
- No. of program/erase cycles : 10,000 (Min)

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

### 3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase data to the flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

### 4. Flash Memory Register

- Flash memory control status register (FMCS)

Address $007A_H$

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| INTE | RDYINT | WE | RDY | Reserved | Reserved | — | Reserved |
| R/W | R/W | R/W | R | R/W | R/W | — | R/W |

Initial value $000X00\text{-}0_B$

## 5. Sector Configuration

The table below shows the sector configuration of flash memory and lists the addresses of each sector during CPU access and a flash memory programming.

• Sector configuration of flash memory

| Flash Memory | CPU Address | Programmer Address* |
|---|---|---|
| 16 K bytes | FFFF$_H$ to C000$_H$ | 1FFFF$_H$ to 1C000$_H$ |
| 8 K bytes | BFFF$_H$ to A000$_H$ | 1BFFF$_H$ to 1A000$_H$ |
| 8 K bytes | 9FFF$_H$ to 8000$_H$ | 19FFF$_H$ to 18000$_H$ |
| 28 K bytes | 7FFF$_H$ to 1000$_H$ | 17FFF$_H$ to 11000$_H$ |

* : The programmer address is the address to be used instead of the CPU address when programming data from a parallel flash memory programmer. Use the programmer address on programming or erasing using a general-purpose programmer.

## 6. ROM Programmer Adaptor and Recommended ROM Programmers

| Package | Applicable adapter model | Recommended writer |
|---|---|---|
| | Sunhayato Corp. | Ando Electric Co. Ltd. |
| FPT-100P-M06 | FLASH-100QF-32DP-8LF2 | AF9708 (ver 1.60 or later) *<br>AF9709 (ver 1.60 or later) * |
| FPT-100P-M05 | FLASH-100SQF-32DP-8LF | |

* : For the programmer and the version of the programmer,contact the Flash Support Group, Inc.

Inquirues : Sunhayato Corp. : TEL : 81-(3)-3984-7791
FAX : 81-(3)-3971-0535
E-mail : adapter@sunhayato.co.jp
Flash Support Group, Inc. : FAX : 81-(53)-428-8377
E-mail : support@j-fsg.co.jp

## ■ PROGRAMMING TO THE EPROM WITH PIGGY-BACK/EVALUATION DEVICE

### 1. EPROM for Use

MBM27C512-20TV

### 2. Programming Socket Adapter

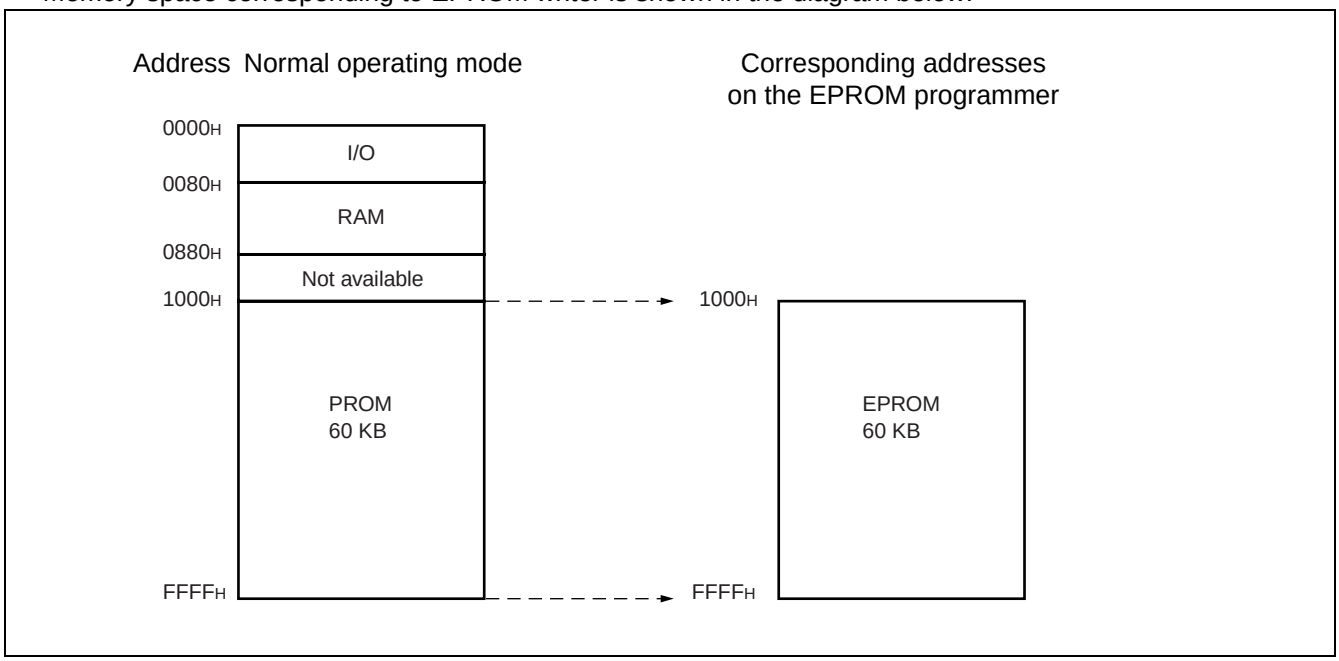
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer : Sunhayato Corp.) .

| Package | Adapter socket part number |
|---|---|
| LCC-32 (Rectangle) | ROM-32LC-28DP-YG |

Inquiry : Sunhayato Corp. : TEL : 81-3-3984-7791
FAX : 81-3-3971-0535
E-mail : adapter@sunhayato.co.jp

### 3. Memory Space

Memory space corresponding to EPROM writer is shown in the diagram below.




### 4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at $1000_H$ to $FFFF_H$.

(3) Program to $1000_H$ to $FFFF_H$ with the EPROM programmer.

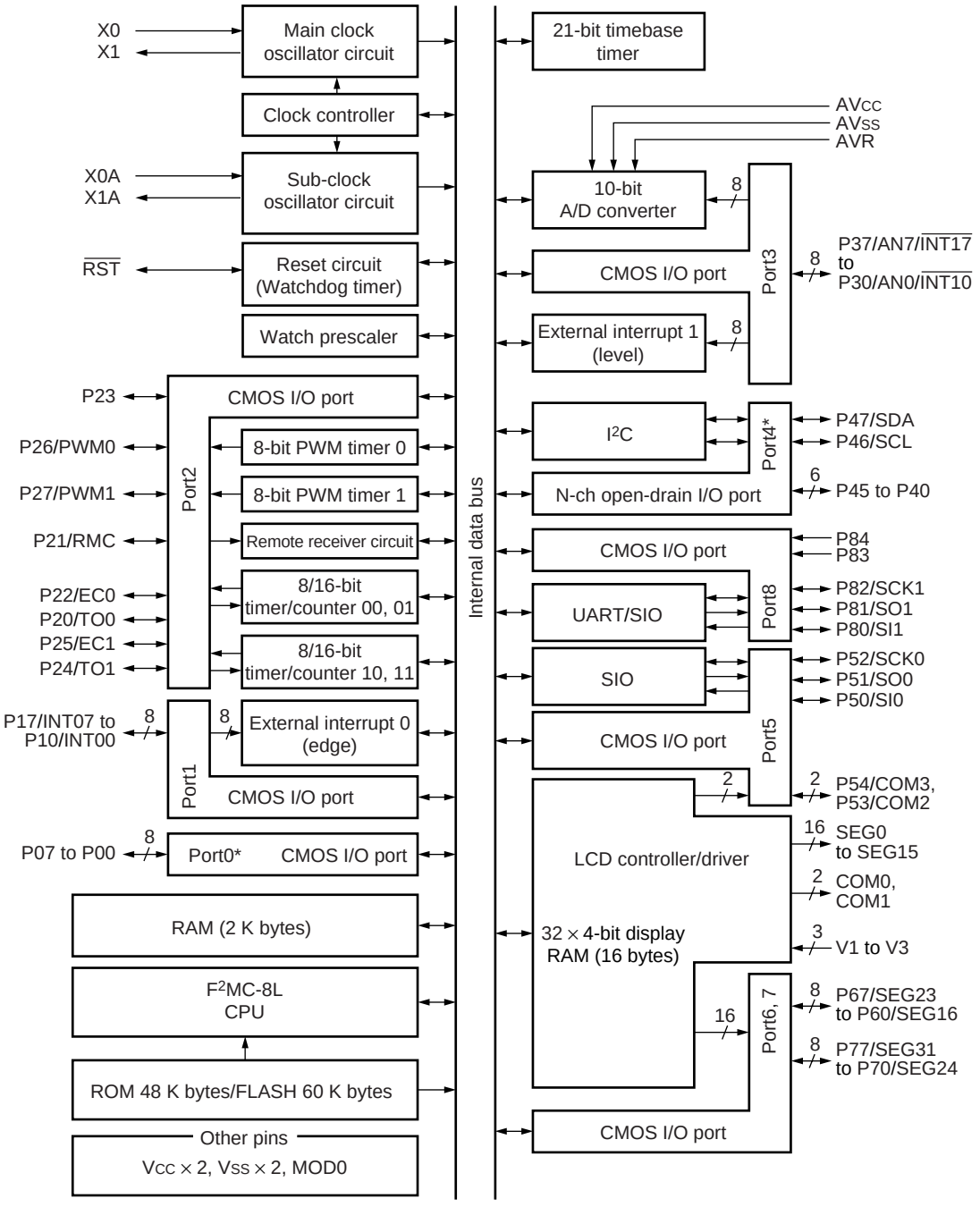
## ■ ICE PROBE POD ADAPTOR OF PIGGY-BACK/EVA CHIP

The following conversion adapter is required to achieve the same pin layout as the FPT-100P-M05.

Adaptor part number: 100QF-100SQF-8L

Inquiry : Sunhayato Corp. : TEL : 81-3-3984-7791
FAX : 81-3-3971-0535
E-mail : adapter@sunhayato.co.jp

## ■ BLOCK DIAGRAM



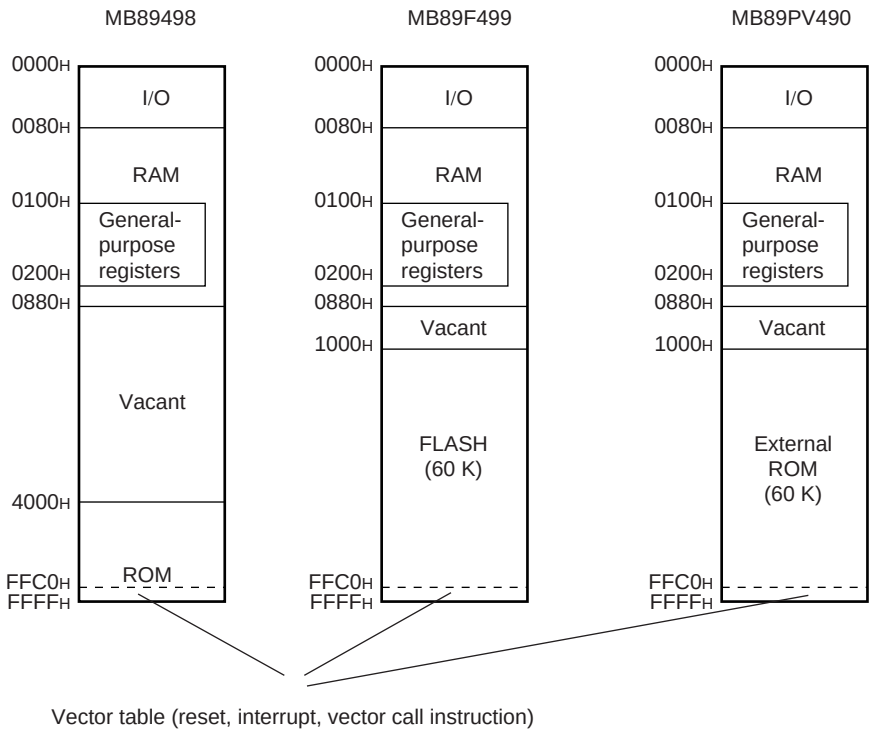

* : High current I/O port.

## ■ CPU CORE

### 1. Memory Space

The microcontrollers of the MB89490 series offer a memory space of 64K bytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt/reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89490 series is structured as illustrated below.

Memory Space



## 2. Registers

The F²MC-8L family has 2 types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided :

Program counter (PC) : A 16-bit register for indicating instruction storage positions.

Accumulator (A) : A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.

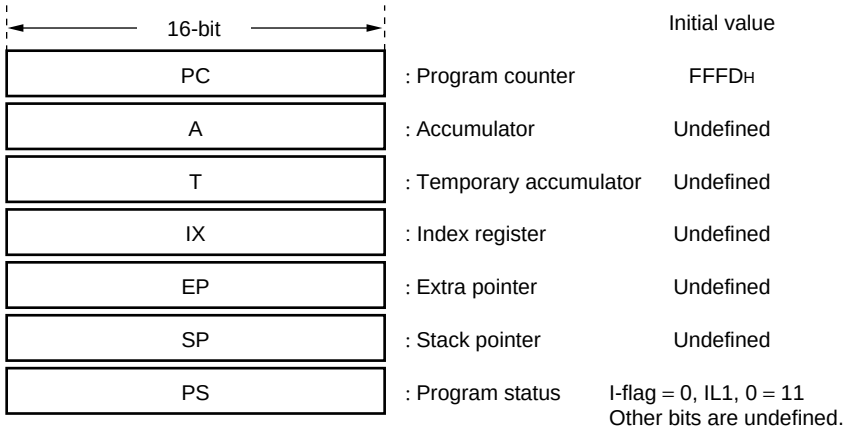
Temporary accumulator (T) : A 16-bit register for performing arithmetic operations with the accumulator. When the instruction is an 8-bit data processing instruction, the lower byte is used.

Index register (IX) : A 16-bit register for index modification.

Extra pointer (EP) : A 16-bit pointer for indicating a memory address.

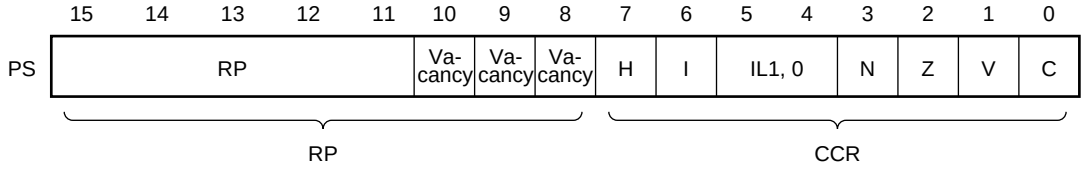
Stack pointer (SP) : A 16-bit register for indicating a stack area.

Program status (PS) : A 16-bit register for storing a register pointer and condition code.



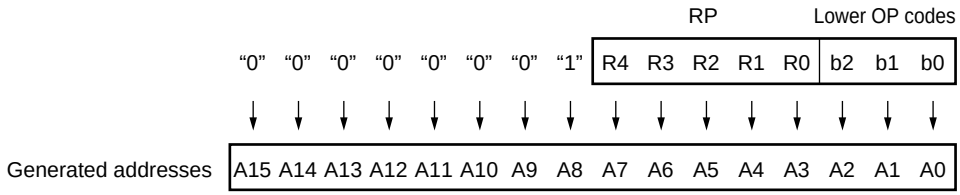

The PS can further be divided into higher 8-bit for use as a register bank pointer (RP) and the lower 8-bit for use as a condition code register (CCR) . (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Conversion rule for Actual Addresses of the General-purpose Register Area




The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for controlling the CPU operations at the time of an interrupt.

H-flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Clear to "0" otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is allowed when this flag is set to "1". Interrupt is prohibited when the flag is set to "0". Clear to "0" at reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request is higher than the value indicated by this bit.

| IL1 | IL0 | Interrupt level | High-low |
|---|---|---|---|
| 0 | 0 | 1 | High ↕ Low |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | |

N-flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Clear to "0" otherwise.

Z-flag : Set to "1" when an arithmetic operation results in "0". Clear to "0" otherwise.

V-flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Clear to "0" if the overflow does not occur.

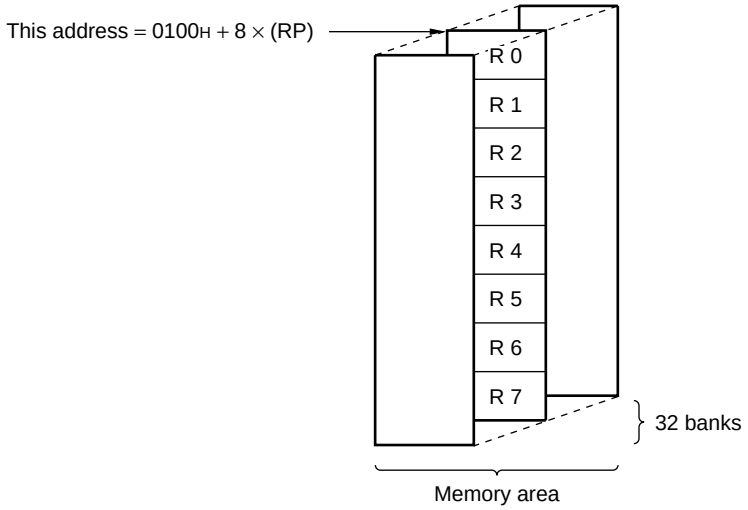
C-flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Clear to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : An 8-bit register for storing data

The general-purpose registers are 8-bit and located in the register banks of the memory.
1 bank contains 8 registers. Up to a total of 32 banks can be used on the MB89490 series. The bank currently in use is indicated by the register bank pointer (RP) .

Register Bank Configuration



## ■ I/O MAP

| Address | Register name | Register description | Read/Write | Initial value |
|---|---|---|---|---|
| $00_H$ | PDR0 | Port 0 data register | R/W | $XXXXXXXX_B$ |
| $01_H$ | DDR0 | Port 0 direction register | W* | $00000000_B$ |
| $02_H$ | PDR1 | Port 1 data register | R/W | $XXXXXXXX_B$ |
| $03_H$ | DDR1 | Port 1 direction register | W* | $00000000_B$ |
| $04_H$ | PDR2 | Port 2 data register | R/W | $00000000_B$ |
| $05_H$ | (Reserved) | | | |
| $06_H$ | DDR2 | Port 2 direction register | R/W | $00000000_B$ |
| $07_H$ | SYCC | System clock control register | R/W | $X\text{-}1MM100_B$ |
| $08_H$ | STBC | Standby control register | R/W | $00010XXX_B$ |
| $09_H$ | WDTC | Watchdog timer control register | W* | $0\text{---}XXXX_B$ |
| $0A_H$ | TBTC | Timebase timer control register | R/W | $00\text{---}000_B$ |
| $0B_H$ | WPCR | Watch prescaler control register | R/W | $00\text{--}0000_B$ |
| $0C_H$ | PDR3 | Port 3 data register | R/W | $XXXXXXXX_B$ |
| $0D_H$ | DDR3 | Port 3 direction register | R/W | $11111111_B$ |
| $0E_H$ | RSFR | Reset flag register | R | $XXXX\text{----}_B$ |
| $0F_H$ | PDR4 | Port 4 data register | R/W | $11111111_B$ |
| $10_H$ | PDR5 | Port 5 data register | R/W | $\text{---}XXXXX_B$ |
| $11_H$ | DDR5 | Port 5 direction register | R/W | $\text{---}00000_B$ |
| $12_H$ | PDR6 | Port 6 data register | R/W | $XXXXXXXX_B$ |
| $13_H$ | DDR6 | Port 6 direction register | R/W | $00000000_B$ |
| $14_H$ | PDR7 | Port 7 data register | R/W | $XXXXXXXX_B$ |
| $15_H$ | DDR7 | Port 7 direction register | R/W | $00000000_B$ |
| $16_H$ | PDR8 | Port 8 data register | R/W | $\text{---}XXXXX_B$ |
| $17_H$ | DDR8 | Port 8 direction register | R/W | $\text{---}00000_B$ |
| $18_H$ | EIC0 | External interrupt 0 control register 0 | R/W | $00000000_B$ |
| $19_H$ | EIC1 | External interrupt 0 control register 1 | R/W | $00000000_B$ |
| $1A_H$ | EIC2 | External interrupt 0 control register 2 | R/W | $00000000_B$ |
| $1B_H$ | EIC3 | External interrupt 0 control register 3 | R/W | $00000000_B$ |
| $1C_H$ | EIE1 | External interrupt 1 enable register | R/W | $00000000_B$ |
| $1D_H$ | EIF1 | External interrupt 1 flag register | R/W | $\text{-------}0_B$ |
| $1E_H$ | SMR | Serial mode register | R/W | $00000000_B$ |
| $1F_H$ | SDR | Serial data register | R/W | $XXXXXXXX_B$ |
| $20_H$ | T01CR | Timer 01 control register | R/W | $000000X0_B$ |
| $21_H$ | T00CR | Timer 00 control register | R/W | $000000X0_B$ |
| $22_H$ | T01DR | Timer 01 data register | R/W | $XXXXXXXX_B$ |

*(Continued)*

| Address | Register name | Register description | Read/Write | Initial value |
|---|---|---|---|---|
| $23_H$ | T00DR | Timer 00 data register | R/W | $XXXXXXXX_B$ |
| $24_H$ | T11CR | Timer 11 control register | R/W | $000000X0_B$ |
| $25_H$ | T10CR | Timer 10 control register | R/W | $000000X0_B$ |
| $26_H$ | T11DR | Timer 11 data register | R/W | $XXXXXXXX_B$ |
| $27_H$ | T10DR | Timer 10 data register | R/W | $XXXXXXXX_B$ |
| $28_H$ | ADER | A/D input enable register | R/W | $11111111_B$ |
| $29_H$ | ADC0 | A/D control register 0 | R/W | $-00000X0_B$ |
| $2A_H$ | ADC1 | A/D control register 1 | R/W | $-0000001_B$ |
| $2B_H$ | ADDH | A/D data register (Upper byte) | R | $------XX_B$ |
| $2C_H$ | ADDL | A/D data register (Lower byte) | R | $XXXXXXXX_B$ |
| $2D_H$ | CNTR0 | PWM 0 timer control register | R/W | $0-000000_B$ |
| $2E_H$ | COMR0 | PWM 0 timer compare register | W* | $XXXXXXXX_B$ |
| $2F_H$ | SMC0 | UART/SIO serial mode control register | R/W | $00000000_B$ |
| $30_H$ | SMC1 | UART/SIO serial mode control register | R/W | $00000000_B$ |
| $31_H$ | SSD | UART/SIO serial status/data register | R/W | $00001---_B$ |
| $32_H$ | SIDR/SODR | UART/SIO serial data register | R/W | $XXXXXXXX_B$ |
| $33_H$ | SRC | UART/SIO serial rate control register | R/W | $XXXXXXXX_B$ |
| $34_H$ | CNTR1 | PWM 1 timer control register | R/W | $0-000000_B$ |
| $35_H$ | COMR1 | PWM 1 timer compare register | W* | $XXXXXXXX_B$ |
| $36_H$ | IBSR | $I^2C$ bus status register | R | $00000000_B$ |
| $37_H$ | IBCR | $I^2C$ bus control register | R/W | $00000000_B$ |
| $38_H$ | ICCR | $I^2C$ clock control register | R/W | $000XXXXX_B$ |
| $39_H$ | IADR | $I^2C$ address register | R/W | $-XXXXXXX_B$ |
| $3A_H$ | IDAR | $I^2C$ data register | R/W | $XXXXXXXX_B$ |
| $3B_H$ | PLLCR | Sub PLL control register | R/W | $----0000_B$ |
| $3C_H$ to $3F_H$ | (Reserved) | | | |
| $40_H$ | RMN | Remote control counter register | R | $XXXXXXXX_B$ |
| $41_H$ | RMC | Remote control control register | R/W | $00000000_B$ |
| $42_H$ | RMS | Remote control status register | R/W | $0X000001_B$ |
| $43_H$ | RMD | Remote control FIFO data register | R | $X----XXX_B$ |
| $44_H$ | RMCD0 | Remote control compare register 0 | R/W | $11111111_B$ |
| $45_H$ | RMCD1 | Remote control compare register 1 | R/W | $11111111_B$ |
| $46_H$ | RMCD2 | Remote control compare register 2 | R/W | $11111111_B$ |
| $47_H$ | RMCD3 | Remote control compare register 3 | R/W | $11111111_B$ |
| $48_H$ | RMCD4 | Remote control compare register 4 | R/W | $11111111_B$ |

*(Continued)*

*(Continued)*

| Address | Register name | Register description | Read/Write | Initial value |
|---|---|---|---|---|
| 49H | RMCD5 | Remote control compare register 5 | R/W | 11111111B |
| 4AH | RMCI | Remote interrupt register | R/W | 0000-000B |
| 4BH to 5DH | (Reserved) | | | |
| 5EH | LOCR | LCD controller output control register | R/W | -0000000B |
| 5FH | LCR | LCD controller control register | R/W | 00010000B |
| 60H to 6FH | VRAM | LCD data RAM | R/W | XXXXXXXXB |
| 70H | PUCR0 | Port 0 pull up resistor control register | R/W | 11111111B |
| 71H | PUCR1 | Port 1 pull up resistor control register | R/W | 11111111B |
| 72H | PUCR2 | Port 2 pull up resistor control register | R/W | 11111111B |
| 73H | PUCR3 | Port 3 pull up resistor control register | R/W | 11111111B |
| 74H | PUCR5 | Port 5 pull up resistor control register | R/W | ---11111B |
| 75H | PUCR6 | Port 6 pull up resistor control register | R/W | 11111111B |
| 76H | PUCR7 | Port 7 pull up resistor control register | R/W | 11111111B |
| 77H | PUCR8 | Port 8 pull up resistor control register | R/W | -----111B |
| 78H to 79H | (Reserved) | | | |
| 7AH | FMCS | Flash memory control status registger | R/W | 000X00-0B |
| 7BH | ILR1 | Interrupt level setting register 1 | W* | 11111111B |
| 7CH | ILR2 | Interrupt level setting register 2 | W* | 11111111B |
| 7DH | ILR3 | Interrupt level setting register 3 | W* | 11111111B |
| 7EH | ILR4 | Interrupt level setting register 4 | W* | 11111111B |
| 7FH | (Reserved) | | | |

* : Bit manipulation instruction cannot be used.

- **Read/write access symbols**
  R/W : Readable and writable
  R : Read-only
  W : Write-only

- **Initial value symbols**
  0 : The initial value of this bit is “0”.
  1 : The initial value of this bit is “1”.
  X : The initial value of this bit is undefined.
  - : Unused bit.
  M : The initial value of this bit is determined by mask option.

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating | | Unit | Remarks |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Power supply voltage*1 | $V_{CC}$<br>$AV_{CC}$ | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | $AV_{CC}$ must be equal to $V_{CC}$ |
| | AVR | $V_{SS}$ – 0.3 | $V_{SS}$ + 4.0 | V | |
| LCD power supply voltage | V1 to V3 | $V_{SS}$ – 0.3 | $V_{CC}$ | V | |
| Input voltage *1 | $V_I$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | Except P40 to P47 |
| | | $V_{SS}$ – 0.3 | $V_{SS}$ + 6.0 | V | P40 to P47 in MB89PV490 and MB89498 |
| | | $V_{SS}$ – 0.3 | $V_{SS}$ + 5.5 | V | P40 to P47 in MB89F499 |
| Output voltage*1 | $V_O$ | $V_{SS}$ – 0.3 | $V_{CC}$ + 0.3 | V | |
| Maximum clamp current | $I_{CLAMP}$ | – 2.0 | + 2.0 | mA | *2 |
| Total maximum clamp current | $\Sigma\|I_{CLAMP}\|$ | — | 20 | mA | *2 |
| “L” level maximum output current | $I_{OL}$ | — | 15 | mA | |
| “L” level average output current | $I_{OLAV}$ | — | 4 | mA | Average value (operating current × operating rate) |
| “L” level total maximum output current | $\Sigma I_{OL}$ | — | 100 | mA | |
| “L” level total average output current | $\Sigma I_{OLAV}$ | — | 40 | mA | Average value (operating current × operating rate) |
| “H” level maximum output current | $I_{OH}$ | — | – 15 | mA | |
| “H” level average output current | $I_{OHAV}$ | — | – 4 | mA | Average value (operating current × operating rate) |
| “H” level total maximum output current | $\Sigma I_{OH}$ | — | – 50 | mA | |
| “H” level total average output current | $\Sigma I_{OHAV}$ | — | – 20 | mA | Average value (operating current × operating rate) |
| Power consumption | $P_D$ | — | 300 | mW | |
| Operating temperature | $T_A$ | – 40 | + 85 | °C | |
| Storage temperature | Tstg | – 55 | + 150 | °C | |

*1 : The parameter is based on $AV_{SS} = V_{SS} = 0.0$ V.

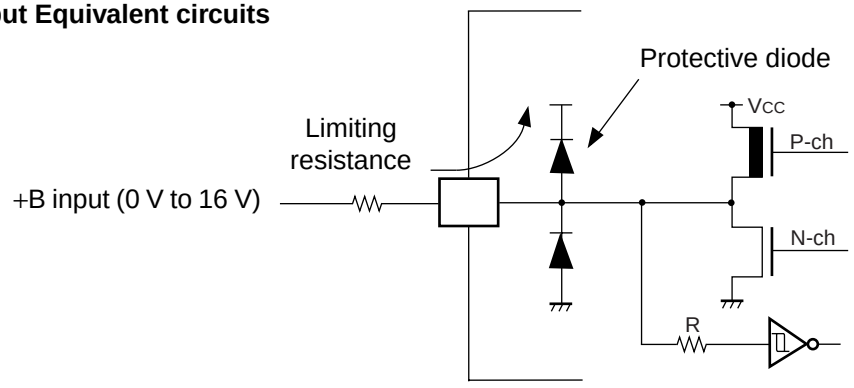
*2 :
- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P52, P80 to P82
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.

*(Continued)*

*(Continued)*

- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

- **Input/Output Equivalent circuits**




WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## 2. Recommended Operating Conditions

($AV_{SS}$ = $V_{SS}$ = 0.0 V)

| Parameter | Symbol | Value | | Unit | Remarks | |
|---|---|---|---|---|---|---|
| | | Min | Max | | | |
| Power supply voltage | $V_{CC}$ $AV_{CC}$ | 2.7* | 3.6 | V | Normal operation assurance range | MB89PV490 and MB89F499 |
| | | 2.2* | 3.6 | V | Normal operation assurance range | MB89498 |
| | | 1.5 | 3.6 | V | Retains the RAM state in stop mode | |
| | AVR | 2.7 | 3.6 | V | | |
| LCD power supply voltage | V1 to V3 | Vss | Vcc | V | | |
| Operating temperature | $T_A$ | –40 | +85 | °C | | |

* : These values depend on the operating conditions and the analog assurance range. See Figure 1, 2 and "5. A/D Converter Electrical Characteristics."

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

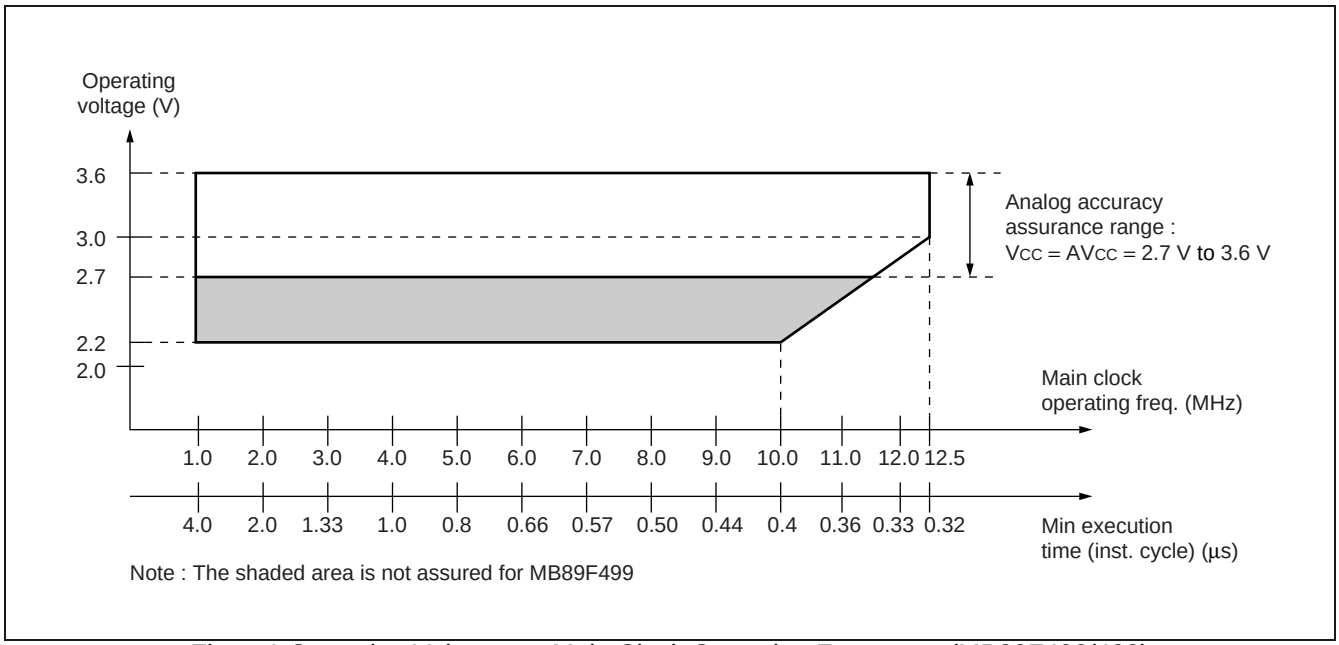

Operating voltage (V)
3.6
3.0
2.7
2.2
2.0
Analog accuracy assurance range : Vcc = AVcc = 2.7 V to 3.6 V
Main clock operating freq. (MHz)
1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 12.5
4.0 2.0 1.33 1.0 0.8 0.66 0.57 0.50 0.44 0.4 0.36 0.33 0.32
Min execution time (inst. cycle) (µs)
Note : The shaded area is not assured for MB89F499

Figure1 Operating Voltage vs. Main Clock Operating Frequency (MB89F499/498)

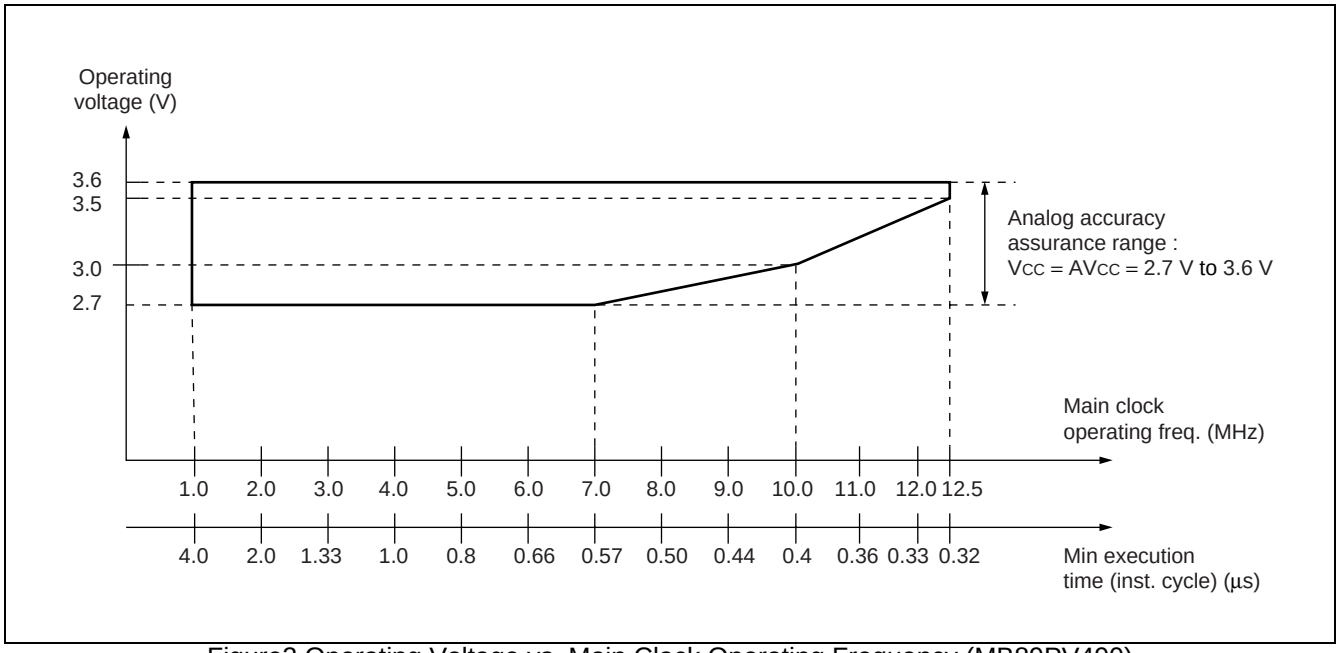



Figure2 Operating Voltage vs. Main Clock Operating Frequency (MB89PV490)

Figure 1 and 2 indicate the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see figure 1 and 2 if the operating speed is switched using a gear.

### 3. DC Characteristics

($AV_{CC} = V_{CC} = 3.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level input voltage | $V_{IH}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P54, P60 to P67, P70 to P77, P80 to P84, SCL, SDA, | — | 0.7 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | | P40 to P47 | — | 0.7 $V_{CC}$ | — | $V_{SS}$ + 6.0 | V | MB89498 |
| | | | — | 0.7 $V_{CC}$ | — | $V_{SS}$ + 5.5 | V | MB89F499 |
| | $V_{IHS}$ | $\overline{RST}$, MOD0, EC0, EC1, SCK0, SI0, SCK1, SI1, RMC, INT00 to INT07 | — | 0.8 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| | $V_{IHA}$ | $\overline{INT10}$ to $\overline{INT17}$ | — | 0.85 $V_{CC}$ | — | $V_{CC}$ + 0.3 | V | |
| "L" level input voltage | $V_{IL}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, P60 to P67, P70 to P77, P80 to P84, SCL, SDA, | — | $V_{SS}$ − 0.3 | — | 0.3 $V_{CC}$ | V | |
| | $V_{ILS}$ | $\overline{RST}$, MOD0, EC0, EC1, SCK0, SI0, SCK1, SI1, RMC, INT00 to INT07 | — | $V_{SS}$ − 0.3 | — | 0.2 $V_{CC}$ | V | |
| | $V_{ILA}$ | $\overline{INT10}$ to $\overline{INT17}$ | — | $V_{SS}$ − 0.3 | — | 0.5 $V_{CC}$ | V | |
| Open-drain output pin application voltage | $V_D$ | P40 to P47 | — | $V_{SS}$ − 0.3 | — | $V_{SS}$ + 6.0 | V | MB89498 |
| | | | — | $V_{SS}$ − 0.3 | — | $V_{SS}$ + 5.5 | V | MB89F499 |

*(Continued)*

($AV_{CC} = V_{CC} = 3.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| "H" level output voltage | $V_{OH}$ | P10 to P17, P20 to P27, P30 to P37, P50 to P54, P60 to P67, P70 to P77, P80 to P82 | $I_{OH} = -2.0$ mA | 2.2 | — | — | V | |
| | | P00 to P07 | $I_{OH} = -4.0$ mA | 2.2 | — | — | V | |
| "L" level output voltage | $V_{OL}$ | P10 to P17, P20 to P27, P30 to P37, P50 to P54, P60 to P67, P70 to P77, P80 to P82, $\overline{RST}$ | $I_{OL} = 4.0$ mA | — | — | 0.4 | V | |
| | | P00 to P07 | $I_{OL} = 12.0$ mA | — | — | 0.4 | V | |
| | | P40 to P47 | $I_{OL} = 15.0$ mA | — | — | 0.4 | V | |
| Input leakage current | $I_{LI}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P54, P60 to P67, P70 to P77, P80 to P84 | $0.45 V < V_I < V_{CC}$ | –5 | — | +5 | µA | Without pull-up resistor |
| Open-drain output leakage current | $I_{LOD}$ | P40 to P47 | $0.0 V < V_I < V_{CC}$ | –5 | — | +5 | µA | |
| Pull-down resistance | $R_{DOWN}$ | MOD0 | $V_I = V_{CC}$ | 25 | 50 | 100 | kΩ | Except MB89F499 |
| Pull-up resistance | $R_{PULL}$ | P00 to P07, P10 to P17, P20 to P27, P30 to P37, P50 to P54, P60 to P67, P70 to P77, P80 to P82, $\overline{RST}$ | $V_I = 0.0$ V | 25 | 50 | 100 | kΩ | When pull-up resistor is selected (except $\overline{RST}$) |
| Common output impedance | $R_{VCOM}$ | COM0 to COM3 | V1 to V3 = +3.0 V | — | — | 2.5 | kΩ | |

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 3.0 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Segment output impedance | $R_{VSEG}$ | SEG0 to SEG31 | V1 to V3 = +3.0 V | — | — | 15 | kΩ | |
| LCD divided resistance | $R_{LCD}$ | — | Between $V_{CC}$ and $V_{SS}$ | 300 | 500 | 750 | kΩ | |
| LCD controller/ driver leakage current | $I_{LCDL}$ | V1 to V3, COM0 to COM3, SEG0 to SEG31 | — | –1 | — | +1 | µA | |
| Power supply current | $I_{CC1}$ | $V_{CC}$ | $F_{CH}$ = 12.5 MHz<br>$t_{inst}$ = 0.33 µs<br>Main clock run mode | — | 8.0 | 12 | mA | MB89F499 |
| | | | | — | 7.0 | 12.0 | mA | MB89498 |
| | $I_{CC2}$ | | $F_{CH}$ = 12.5 MHz<br>$t_{inst}$ = 5.33 µs<br>Main clock run mode | — | 1.0 | 3.0 | mA | MB89F499<br>MB89498 |
| | $I_{CCS1}$ | | $F_{CH}$ = 12.5 MHz<br>$t_{inst}$ = 0.33 µs<br>Main clock sleep mode | — | 3.0 | 5.0 | mA | MB89F499<br>MB89498 |
| | $I_{CCS2}$ | | $F_{CH}$ = 12.5 MHz<br>$t_{inst}$ = 5.33 µs<br>Main clock sleep mode | — | 0.6 | 2.0 | mA | MB89F499<br>MB89498 |
| | $I_{CCL}$ | | $F_{CL}$ = 32.768 kHz<br>Sub-clock mode<br>$T_A$ = +25 °C | — | 40.0 | 60.0 | µA | MB89F499<br>MB89498 |
| | $I_{CCLPLL}$ | | $F_{CL}$ = 32.768 kHz<br>Sub-clock mode<br>$T_A$ = +25 °C<br>sub PLL × 4 | — | 180.0 | 250.0 | µA | MB89F499<br>MB89498 |
| | $I_{CCLS}$ | | $F_{CL}$ = 32.768 kHz<br>Sub-clock sleep mode<br>$T_A$ = +25 °C | — | 14.0 | 30.0 | µA | MB89F499<br>MB89498 |
| | $I_{CCT}$ | | $F_{CL}$ = 32.768 kHz<br>Watch mode<br>Main clock stop mode<br>$T_A$ = +25 °C | — | 1.5 | 13.0 | µA | MB89F499<br>MB89498 |

*(Continued)*

*(Continued)*

($AV_{CC}$ = $V_{CC}$ = 3.0 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Power supply current | $I_{CCH}$ | $V_{CC}$ | $T_A$ = +25 °C<br>Sub-clock stop mode | — | 0.8 | 4.0 | µA | MB89F499<br>MB89498 |
| | $I_A$ | $AV_{CC}$ | $AV_{CC}$ = 3.0 V,<br>$T_A$ = +25 °C | — | 1.2 | 4.4 | mA | A/D converting |
| | $I_{AH}$ | | $T_A$ = +25 °C | — | 0.8 | 4.0 | µA | A/D stop |
| Input capacitance | $C_{IN}$ | Except $V_{CC}$, $V_{SS}$, $AV_{CC}$, $AV_{SS}$, AVR | f = 1 MHz | — | 10.0 | — | pF | |

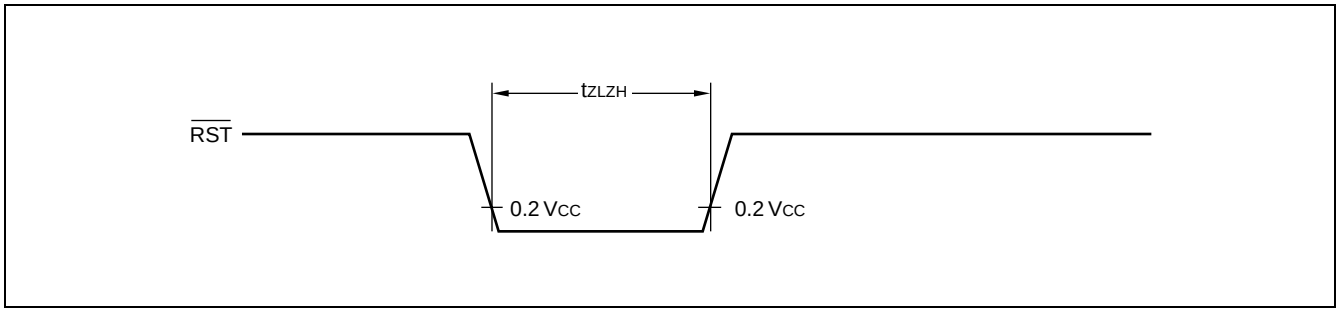
## 4. AC Characteristics

### (1) Reset Timing

($AV_{CC}$ = $V_{CC}$ = 3.0 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $\overline{RST}$ "L" pulse width | $t_{ZLZH}$ | — | 48 $t_{HCYL}$ | — | ns | |

Note : $t_{HCYL}$ is the oscillation cycle ($1/F_{CH}$) to input to the X0 pin.
The MCU operation is not guaranteed when the "L" pulse width is shorter than $t_{ZLZH}$.

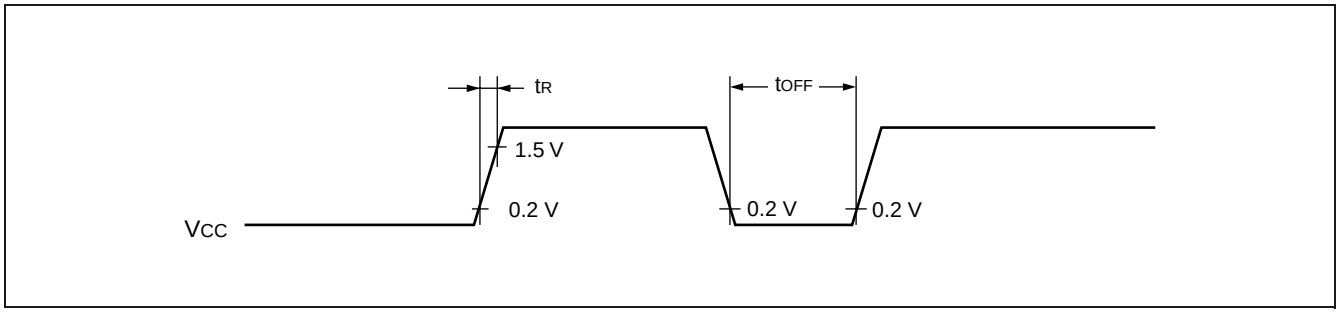



### (2) Power-on Reset

($AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Power supply rising time | $t_R$ | — | — | 50 | ms | |
| Power supply cut-off time | $t_{OFF}$ | | 1 | — | ms | Due to repeated operations |

Note : Make sure that power supply rises within the selected oscillation stabilization time.
Rapid changes in power supply voltage may cause a power-on reset. If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

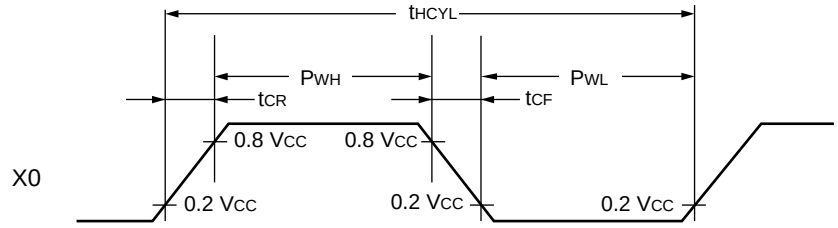


### (3) Clock Timing

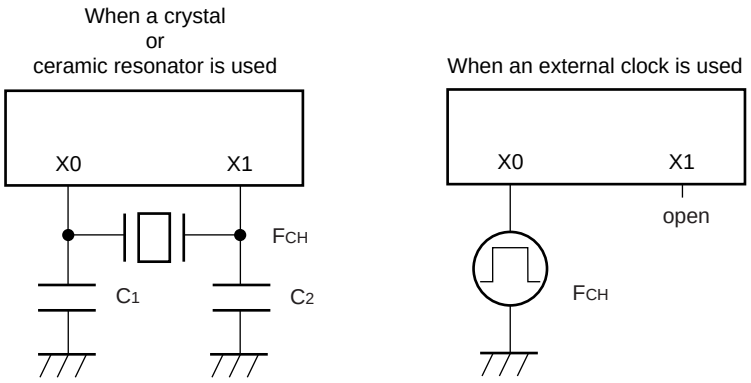
($AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Clock frequency | $F_{CH}$ | X0, X1 | 1 | — | 12.5 | MHz | |
| | $F_{CL}$ | X0A, X1A | — | 32.768 | 75 | kHz | |
| Clock cycle time | $t_{HCYL}$ | X0, X1 | 80 | — | 1000 | ns | |
| | $t_{LCYL}$ | X0A, X1A | 13.3 | 30.5 | — | µs | |
| Input clock pulse width | $P_{WH}$<br>$P_{WL}$ | X0 | 20 | — | — | ns | External clock |
| | $P_{WHL}$<br>$P_{WLL}$ | X0A | — | 15.2 | — | µs | |
| Input clock rising/falling time | $t_{CR}$<br>$t_{CF}$ | X0, X0A | — | — | 10 | ns | |

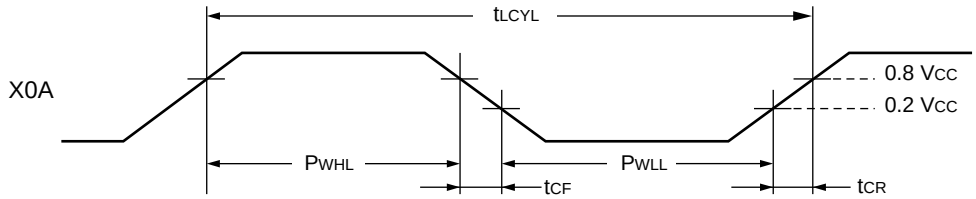
X0 and X1 Timing and Conditions



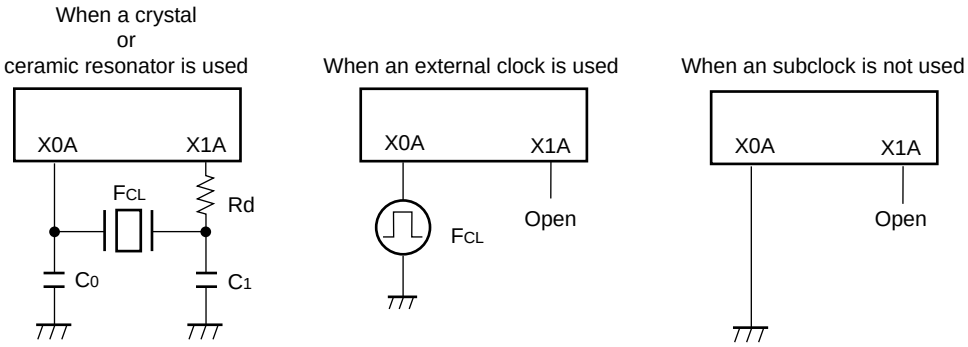

Main Clock Conditions



Sub-clock Timing and Conditions




Sub-clock Conditions

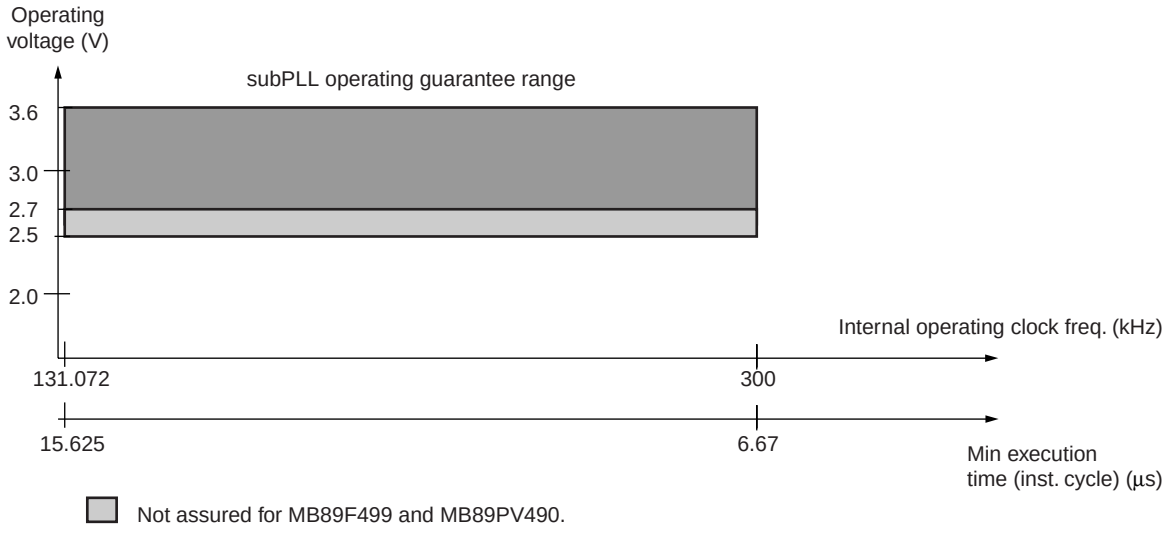



**(4) Instruction Cycle**

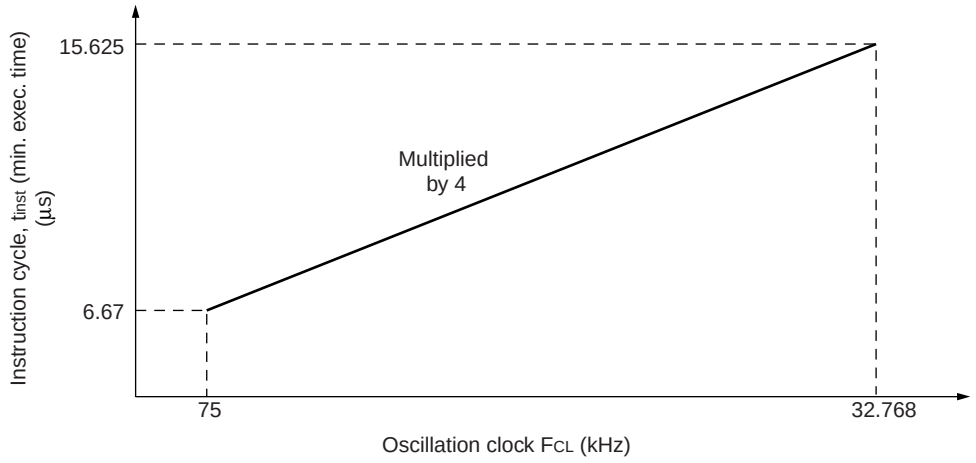
| Parameter | Symbol | Value (typical) | Unit | Remarks |
|---|---|---|---|---|
| Instruction cycle (minimum execution time) | $t_{inst}$ | $4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$ | µs | $(4/F_{CH})$ $t_{inst}$ = 0.32 µs when operating at $F_{CH}$ = 12.5 MHz |
| | | $2/F_{CL}$, $1/2F_{CL}$ | µs | $(2/F_{CL})$ $t_{inst}$ = 61.036 µs when operating at $F_{CL}$ = 32.768 kHz |

- PLL operation guarantee range (sub PLL × 4)

Relationship between internal operating clock frequency and power supply voltage




Relationship between sub-clock oscillating frequency and instruction cycle when sub PLL is enabled



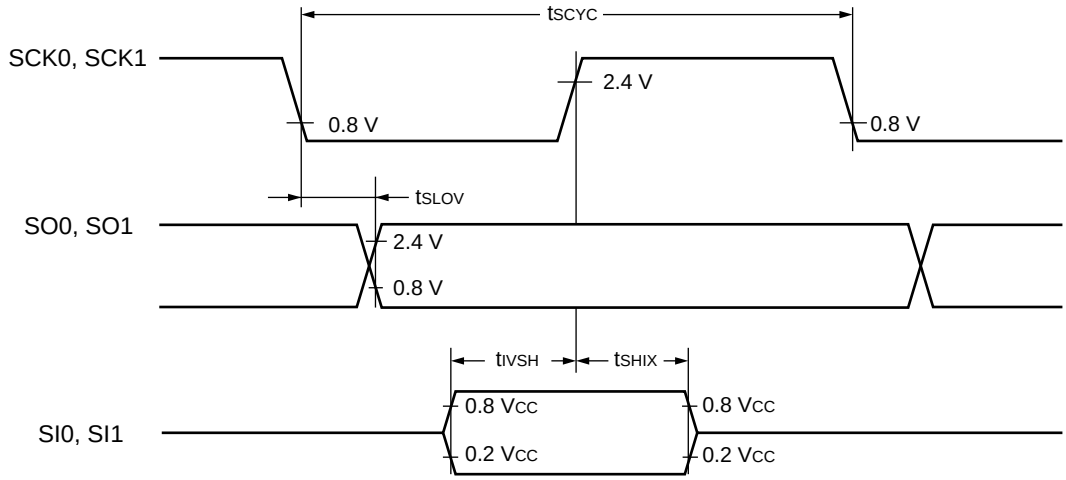
### (5) Serial I/O Timing

($AV_{CC}$ = $V_{CC}$ = 3.0 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

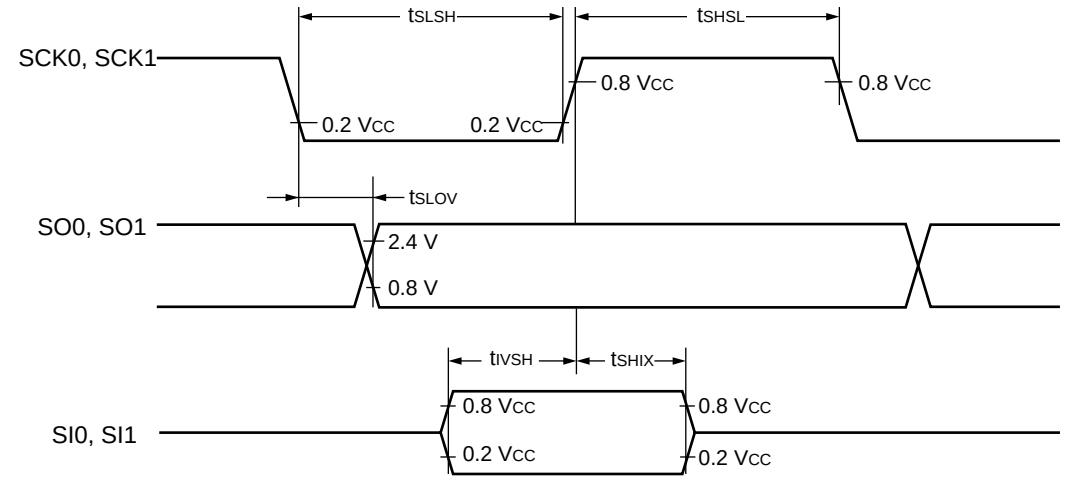
| Parameter | Symbol | Pin | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0, SCK1 | Internal shift clock mode | 2 $t_{inst}$* | — | µs |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK0, SCK1, SO0, SO1 | | –200 | 200 | ns |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SI0, SI1, SCK0, SCK1 | | 1/2 $t_{inst}$* | — | µs |
| SCK ↑ → valid SI hold time | $t_{SHIX}$ | SCK0, SCK1, SI0, SI1 | | 1/2 $t_{inst}$* | — | µs |
| Serial clock “H” pulse width | $t_{SHSL}$ | SCK0, SCK1 | External shift clock mode | 1 $t_{inst}$* | — | µs |
| Serial clock “L” pulse width | $t_{SLSH}$ | | | 1 $t_{inst}$* | — | µs |
| SCK ↓ → SO time | $t_{SLOV}$ | SCK0, SCK1, SO0, SO1 | | 0 | 200 | ns |
| Valid SI → SCK ↑ | $t_{IVSH}$ | SI0, SI1, SCK0, SCK1 | | 1/2 $t_{inst}$* | — | µs |
| SCK ↑ → valid SI hold time | $t_{SHIX}$ | SCK0, SCK1, SI0, SI1 | | 1/2 $t_{inst}$* | — | µs |

* : For information on $t_{inst}$, see “ (4)  Instruction Cycle.”

Internal Clock Operation




External Clock Operation



**(6) I²C Timing**

($V_{CC}$ = 3.0V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Start condition output | $t_{STA}$ | SCL SDA | 1/4 $t_{inst}$*1 × M × N – 20 | 1/4 $t_{inst}$ × M × N + 20 | ns | At master mode |
| Stop condition output | $t_{STO}$ | SCL SDA | 1/4 $t_{inst}$ × (M × N + 8) – 20 | 1/4 $t_{inst}$ × (M*2 × N*3 + 8) + 20 | ns | At master mode |
| Start condition detect | $t_{STA}$ | SCL SDA | 1/4 $t_{inst}$ × 6 + 40 | — | ns | |
| Stop condition detect | $t_{STO}$ | SCL SDA | 1/4 $t_{inst}$ × 6 + 40 | — | ns | |
| Re-start condition output | $t_{STASU}$ | SCL SDA | 1/4 $t_{inst}$ × (M × N + 8) – 20 | 1/4 $t_{inst}$ × (M × N + 8) + 20 | ns | At master mode |
| Re-start condition detect | $t_{STASU}$ | SCL SDA | 1/4 $t_{inst}$ × 4 + 40 | — | ns | |
| SCL output LOW width | $t_{LOW}$ | SCL | 1/4 $t_{inst}$ × M × N – 20 | 1/4 $t_{inst}$ × M × N + 20 | ns | At master mode |
| SCL output HIGH width | $t_{HIGH}$ | SCL | 1/4 $t_{inst}$ × (M × N + 8) – 20 | 1/4 $t_{inst}$ × (M × N + 8) + 20 | ns | At master mode |
| SDA output delay | $t_{DO}$ | SDA | 1/4 $t_{inst}$ × 4 – 20 | 1/4 $t_{inst}$ × 4 + 20 | ns | |
| SDA output setup time after interrupt | $t_{DOSU}$ | SDA | 1/4 $t_{inst}$ × 4 – 20 | — | ns | *4 |
| SCL input LOW pulse width | $t_{LOW}$ | SCL | 1/4 $t_{inst}$ × 6 + 40 | — | ns | |
| SCL input HIGH pulse width | $t_{HIGH}$ | SCL | 1/4 $t_{inst}$ × 2 + 40 | — | ns | |
| SDA input setup time | $t_{SU}$ | SDA | 40 | — | ns | |
| SDA hold time | $t_{HO}$ | SDA | 0 | — | ns | |

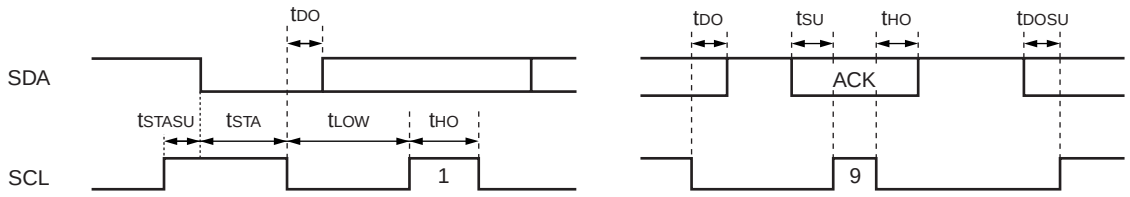
*1 : For information in $t_{inst}$, see “ (4) Instruction Cycle”.

*2 : M is defined in the I²C clock control register ICCR bit 4 and bit 3 (CS4 and CS3). For details, please refer to the H/W manual register explanation.

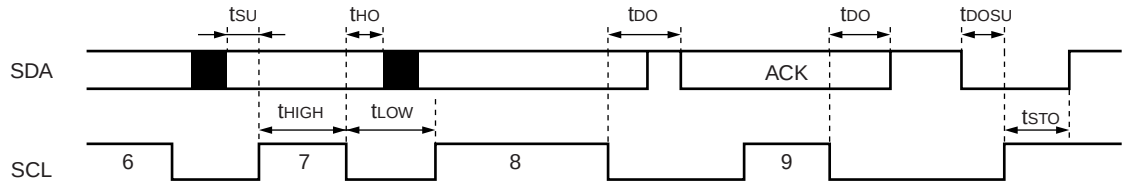
*3 : N is defined in the I²C clock control register ICCR bit 2 to bit 0 (CS2 to CS0).

*4 : When the interrupt period is greater than SCL “L” width, SDA and SCL output (Standard) value is based on hypothesis when rising time is 0 ns.

Data transmit (master/slave)




Data receive (master/slave)

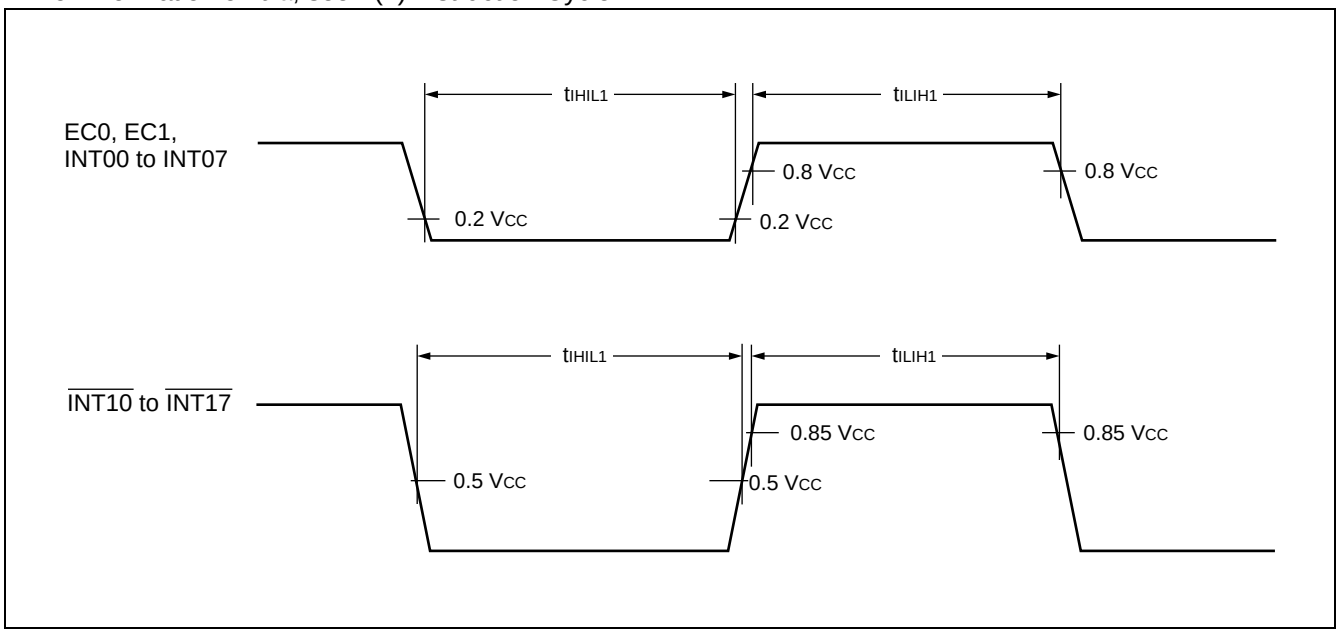


### (7) Peripheral Input Timing

($AV_{CC} = V_{CC} = 3.0$ V, $AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40$ °C to +85 °C)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Peripheral input “H” pulse width 1 | $t_{ILIH1}$ | EC0, EC1, INT00 to INT07, $\overline{INT10}$ to $\overline{INT17}$ | 2 $t_{inst}$* | — | µs | |
| Peripheral input “L” pulse width 1 | $t_{IHIL1}$ | | 2 $t_{inst}$* | — | µs | |

* : For information on $t_{inst}$, see “ (4) Instruction Cycle.”



## 5. A/D Converter Electrical Characteristics

### (1) A/D Converter Electrical Characteristics

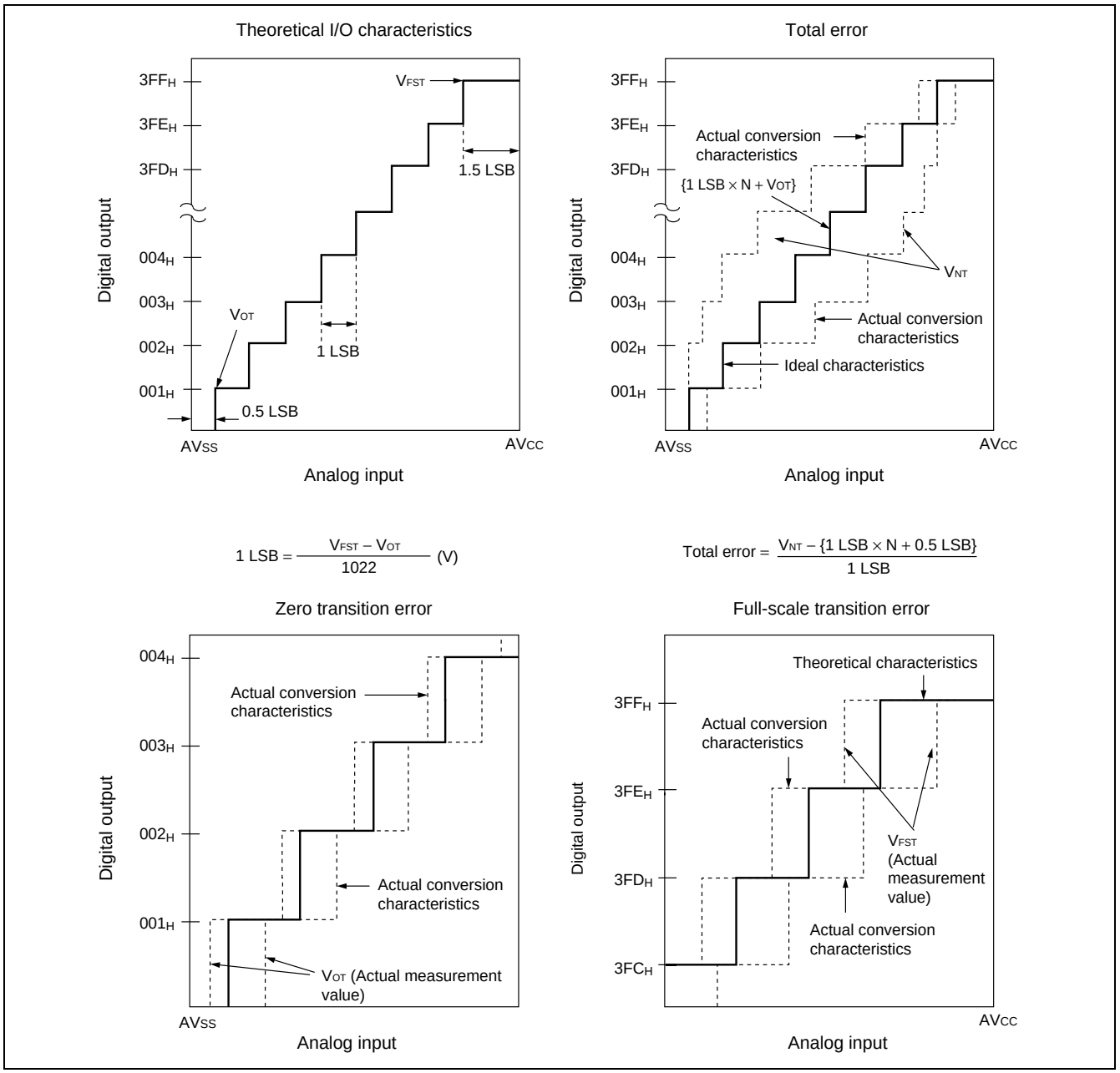
($AV_{CC}$ = $V_{CC}$ = 2.7 V to 3.6 V, $AV_{SS}$ = $V_{SS}$ = 0.0 V, $T_A$ = –40 °C to +85 °C)

| Parameter | Symbol | Pin | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | 10 | — | bit | |
| Total error | | | — | — | ±3.0 | LSB | |
| Linearity error | | | — | — | ±2.5 | LSB | |
| Differential linearity error | | | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | | $AV_{SS}$ – 1.5 LSB | $AV_{SS}$ + 0.5 LSB | $AV_{SS}$ + 2.5 LSB | mV | |
| Full-scale transition voltage | $V_{FST}$ | | $AV_{CC}$ – 3.5 LSB | $AV_{CC}$ – 1.5 LSB | $AV_{CC}$ – 0.5 LSB | mV | |
| A/D mode conversion time | — | | 30 $t_{inst}$* | — | — | µs | |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | — | — | 10 | µA | |
| Analog input voltage | $V_{AIN}$ | | $AV_{SS}$ | — | AVR | V | |
| Reference voltage | — | AVR | $AV_{SS}$ + 2.7 | — | $AV_{CC}$ | V | |
| Reference voltage supply current | $I_R$ | | — | 95.0 | 170.0 | µA | A/D is activated |
| | $I_{RH}$ | | — | — | 4.0 | µA | A/D is stopped |

* : For information on $t_{inst}$, see “ (4) Instruction Cycle” in “4. AC Characteristics”.

**(2) A/D Converter Glossary**

- Resolution
  Analog changes that are identifiable with the A/D converter.
  When the number of bits is 10, analog voltage can be divided into $2^{10} = 1024$.
- Linearity error (unit : LSB)
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics.
- Differential linearity error (unit : LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value.
- Total error (unit : LSB)
  The difference between theoretical and actual conversion values.

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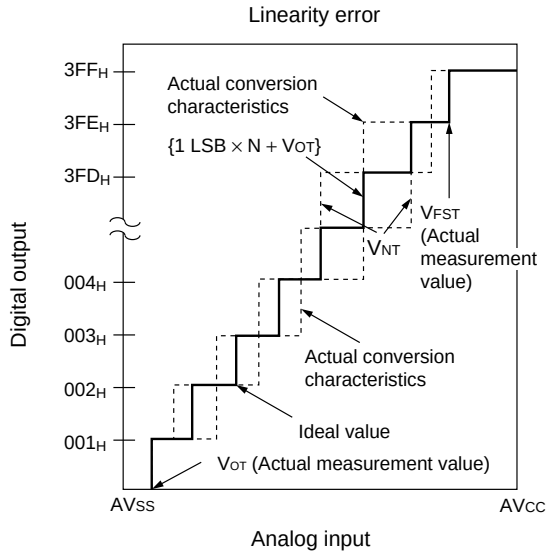
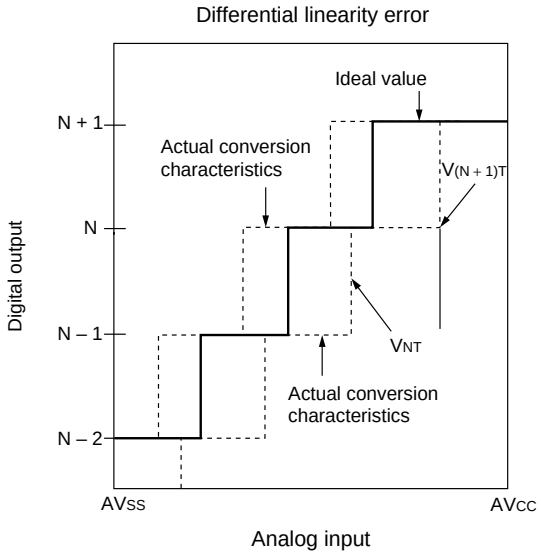



$$\text{Linearity error} = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

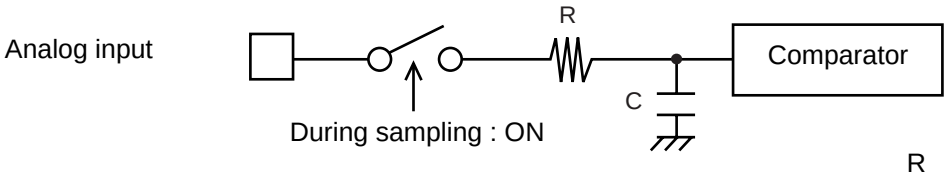
$$\text{Differential linearity error} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

### (3) Notes on Using A/D Converter

**● About the external impedance of the analog input and its sampling time**

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

● Analog input circuit model



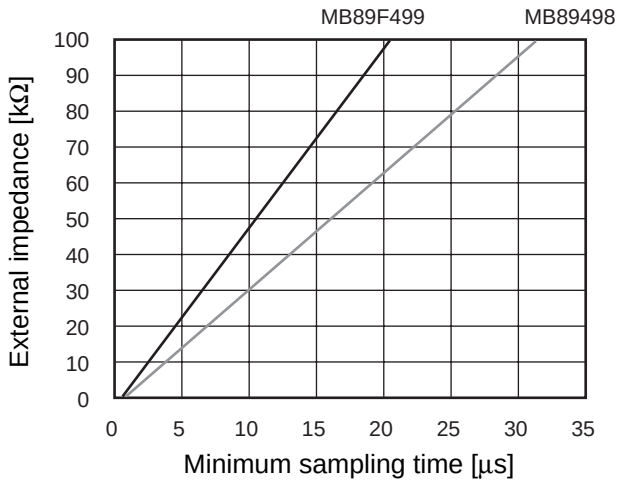

| | R | C |
|---|---|---|
| MB89498 | 2.4 kΩ (Max) | 44.0 pF (Max) |
| MB89F499 | 2.4 kΩ (Max) | 28.6 pF (Max) |

Note : The values are reference values.

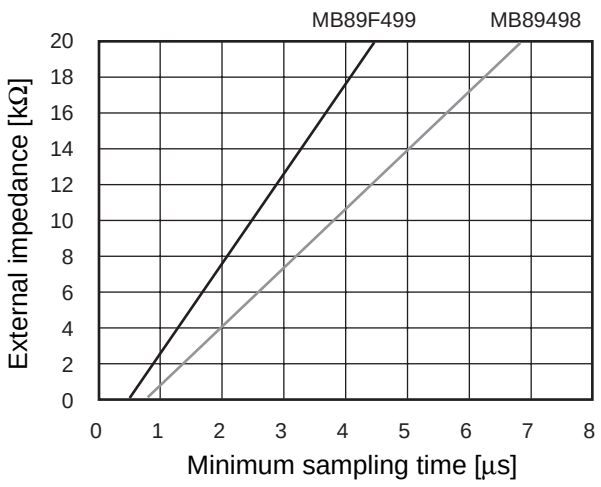
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

● The relationship between external impedance and minimum sampling time

(External impedance = 0 kΩ to 100 kΩ)




(External impedance = 0 kΩ to 20 kΩ)



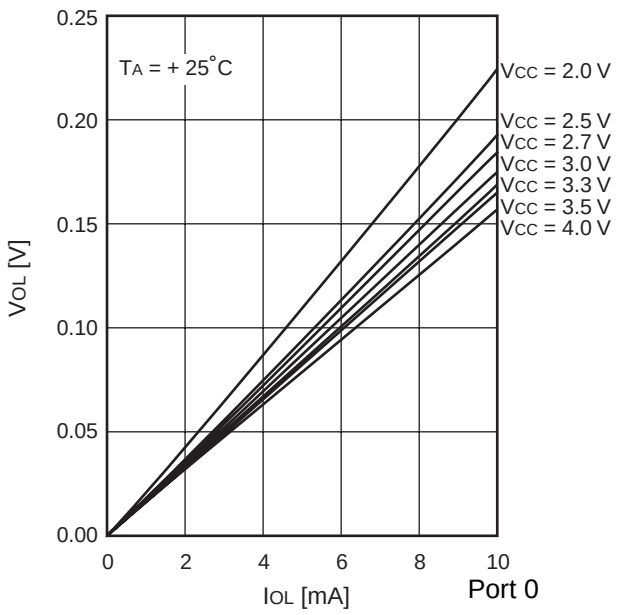

- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

- About errors
  As |AVRH − $AV_{SS}$| becomes smaller, values of relative errors grow larger.

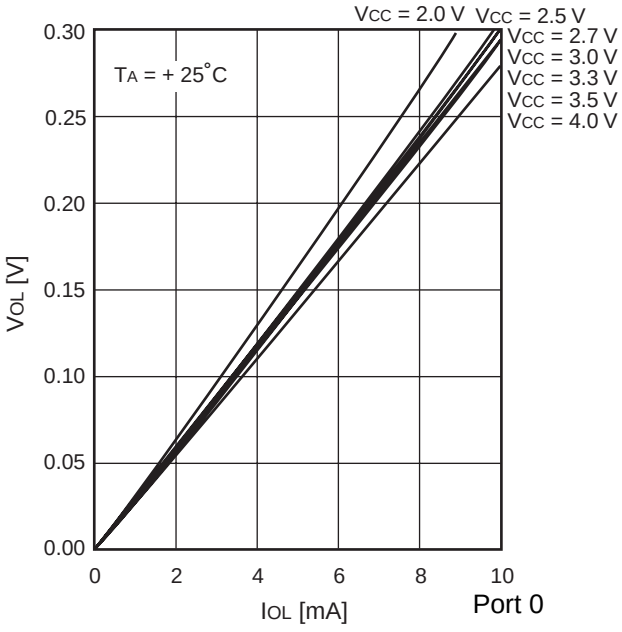
## ■ EXAMPLE CHARACTERISTICS

**(1) “L” level output voltage**

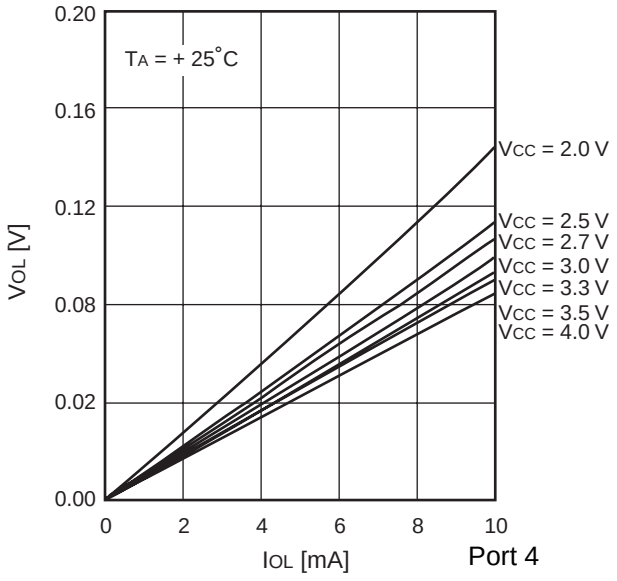
$V_{OL}$ vs $I_{OL}$ (MB89498)



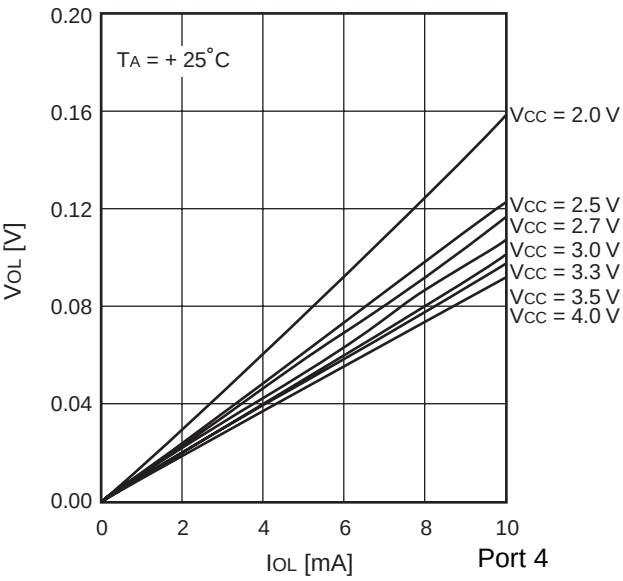

$V_{OL}$ vs $I_{OL}$ (MB89F499)




$V_{OL}$ vs $I_{OL}$ (MB89498)




$V_{OL}$ vs $I_{OL}$ (MB89F499)

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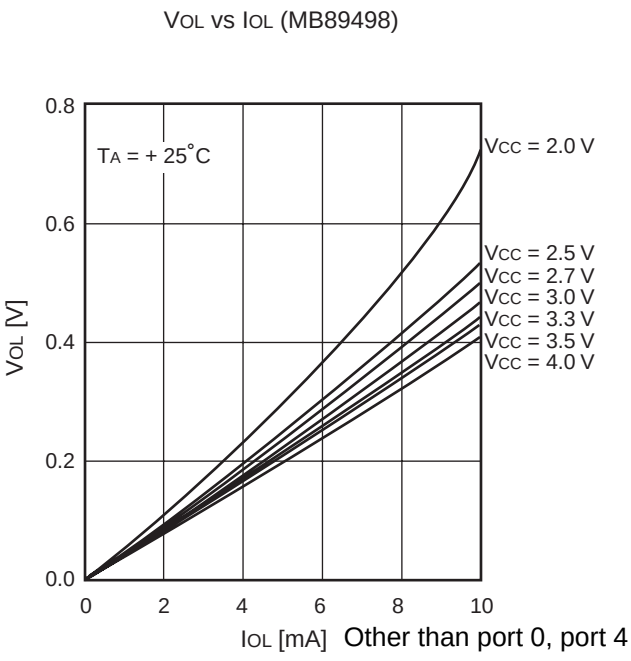
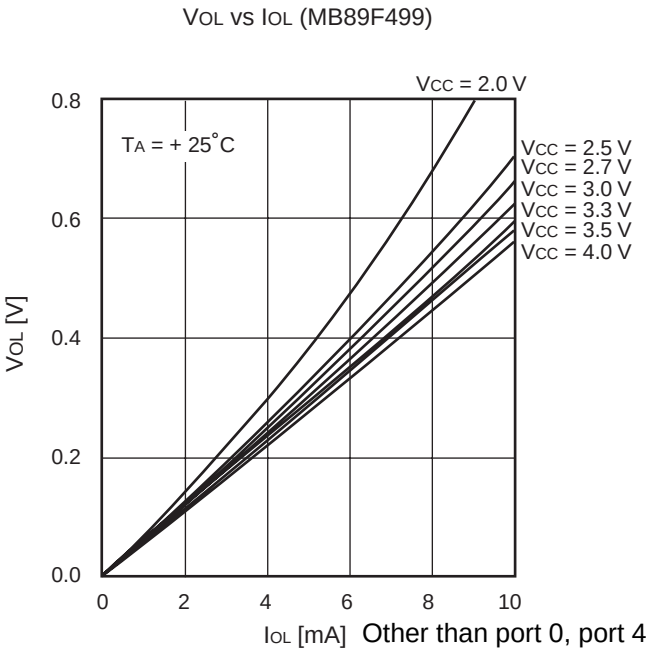
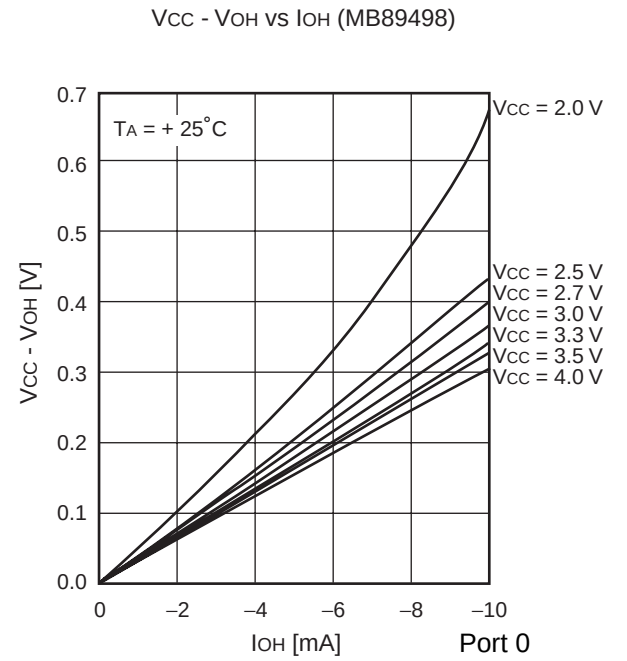
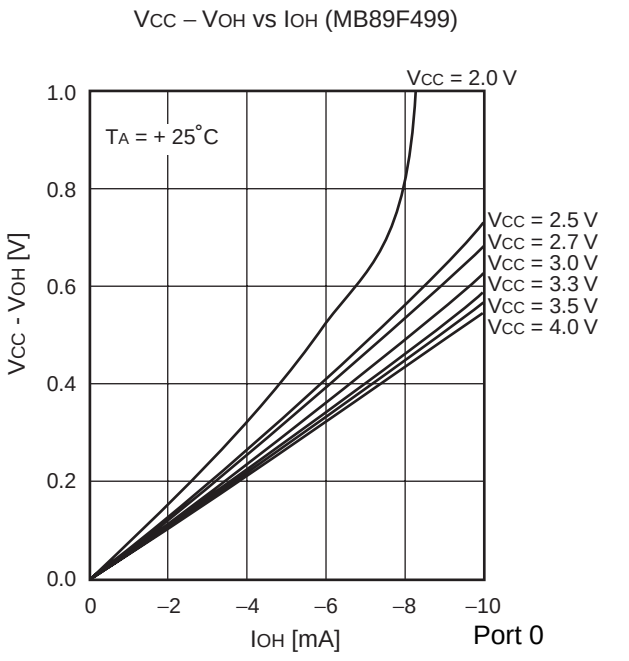



**(2) “H” level output voltage**

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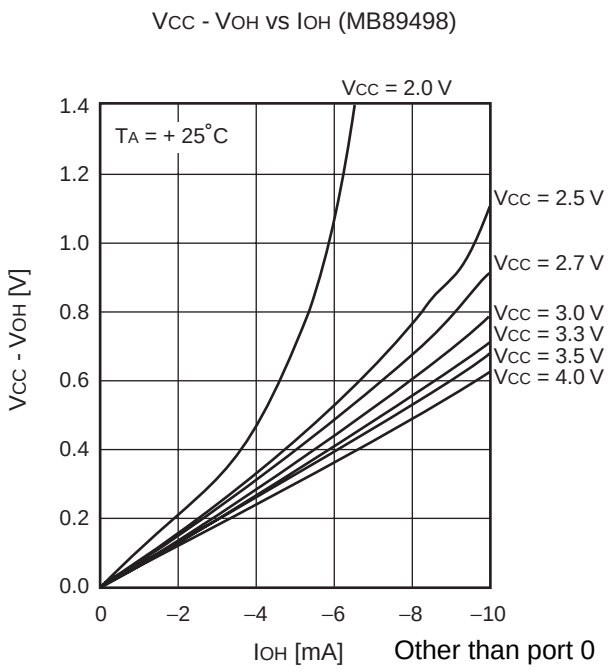
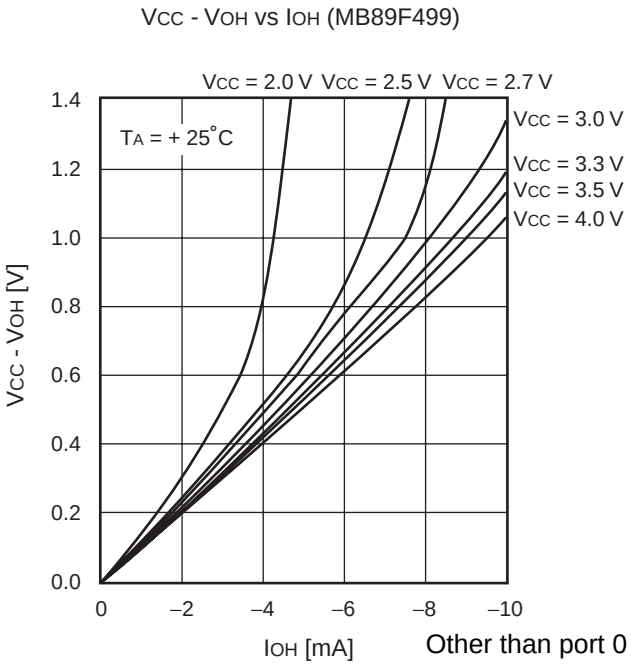
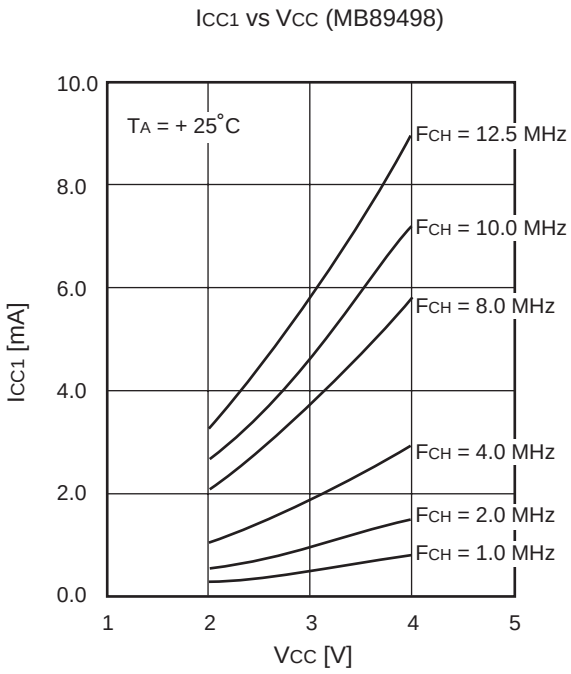
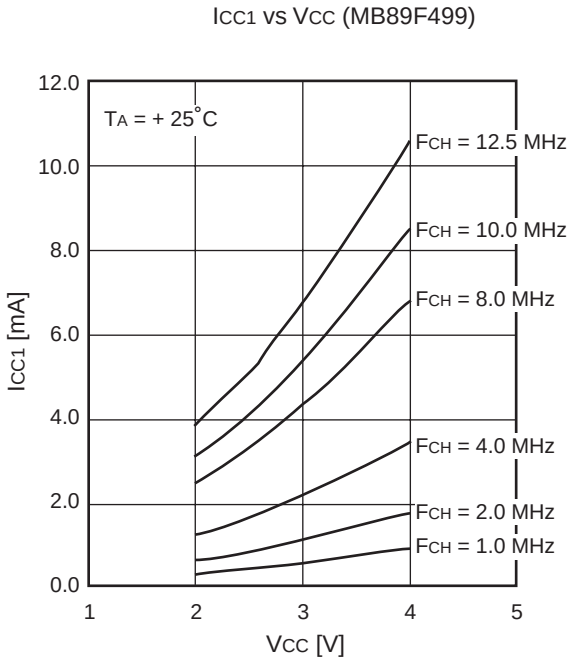


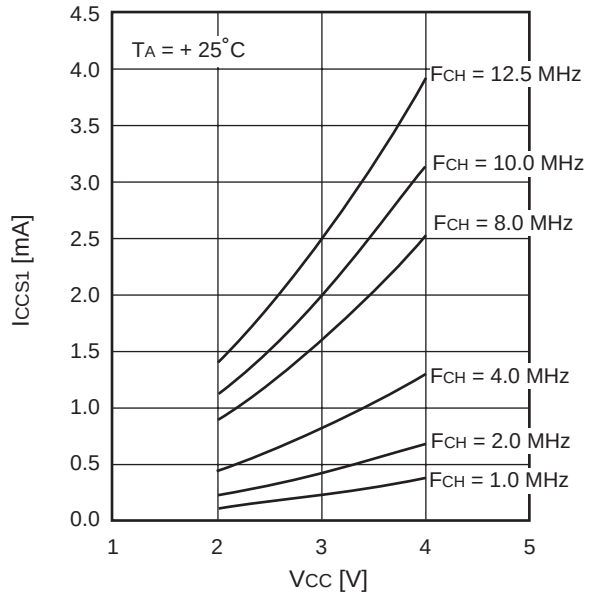

**(3) Power supply current (External clock)**



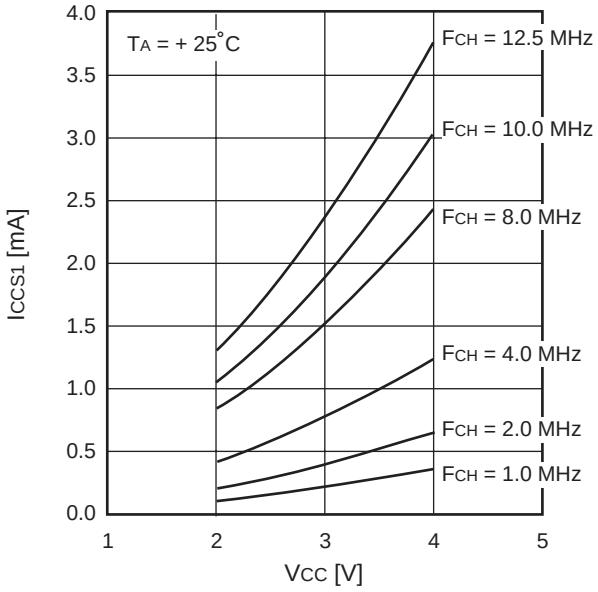




*(Continued)*

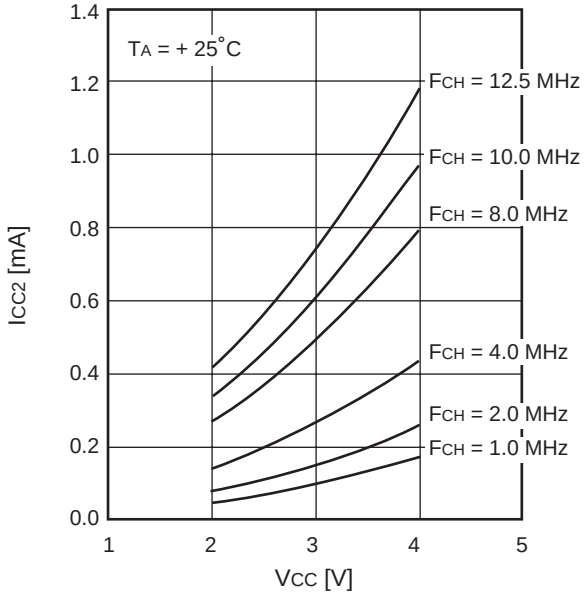
$I_{CCS1}$ vs $V_{CC}$ (MB89498)



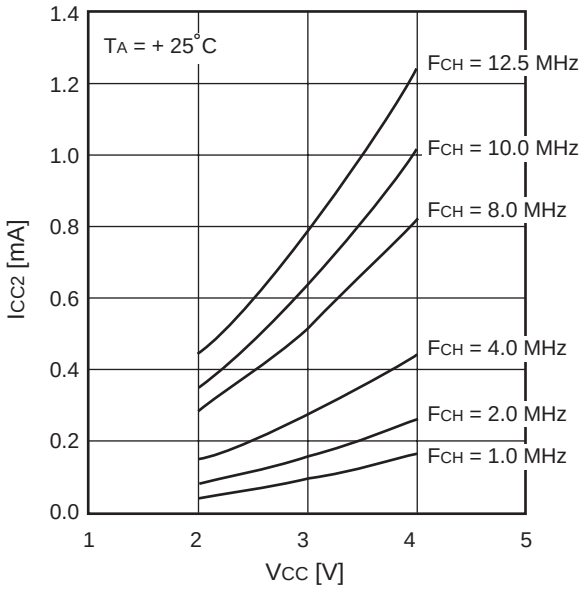

$I_{CCS1}$ vs $V_{CC}$ (MB89F499)




$I_{CC2}$ vs $V_{CC}$ (MB89498)




$I_{CC2}$ vs $V_{CC}$ (MB89F499)

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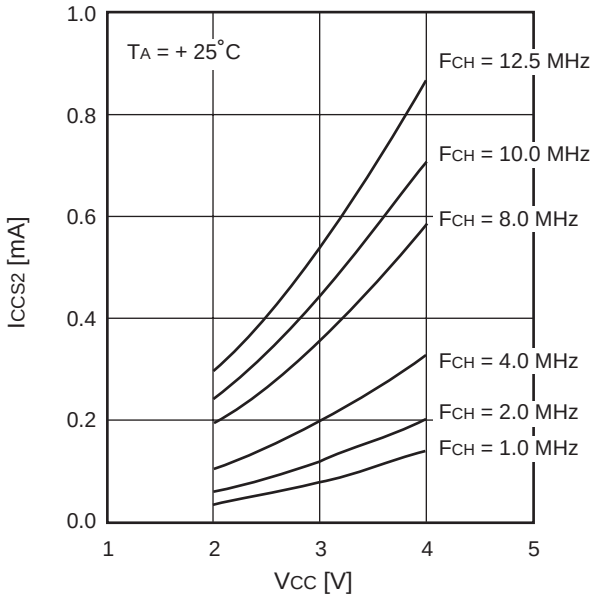
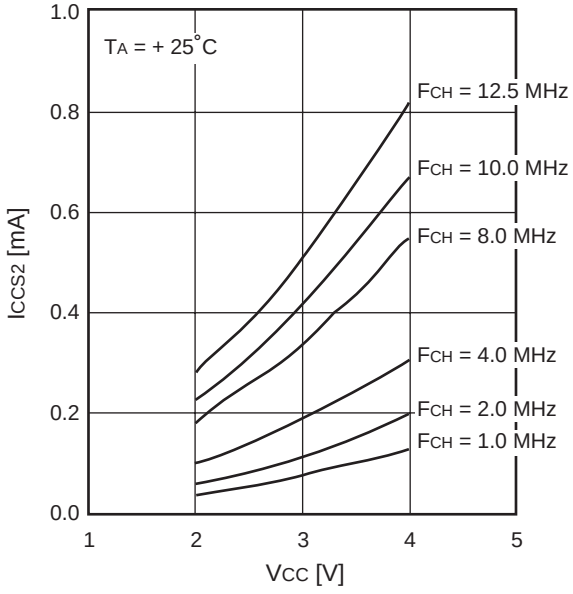
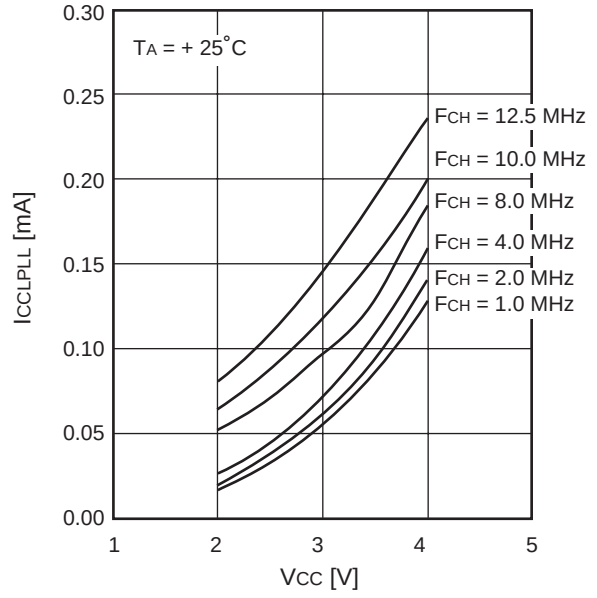
ICCS2 vs VCC (MB89498)



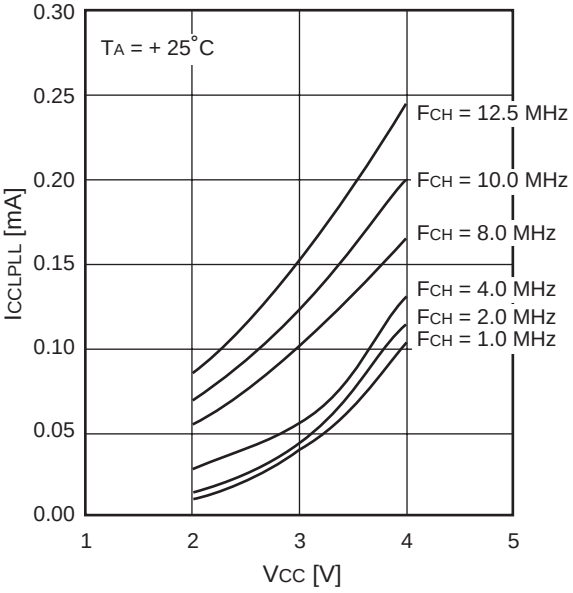

ICCS2 vs VCC (MB89F499)




ICCLPLL vs VCC (MB89498)




ICCLPLL vs VCC (MB89F499)

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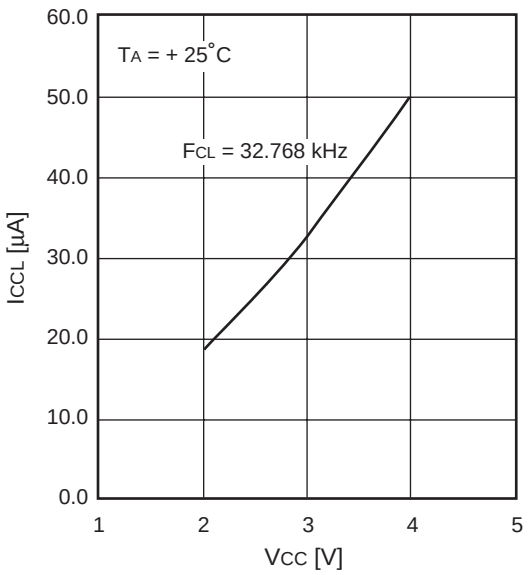
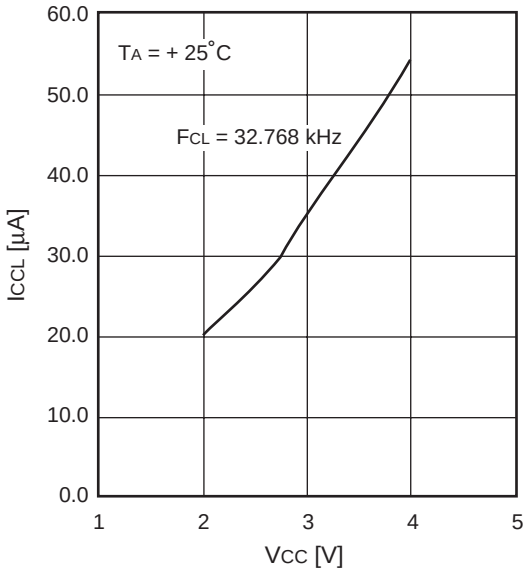
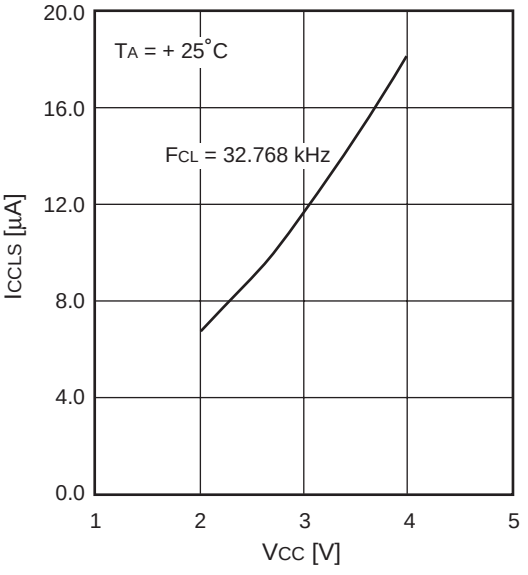
$I_{CCL}$ vs $V_{CC}$ (MB89498)



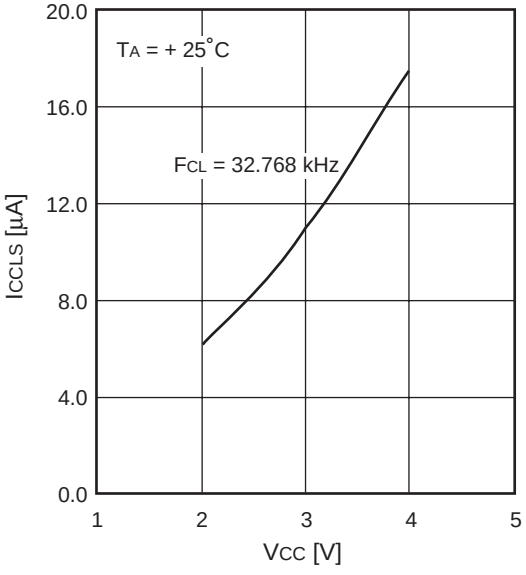

$I_{CCL}$ vs $V_{CC}$ (MB89F499)




$I_{CCLS}$ vs $V_{CC}$ (MB89498)




$I_{CCLS}$ vs $V_{CC}$ (MB89F499)

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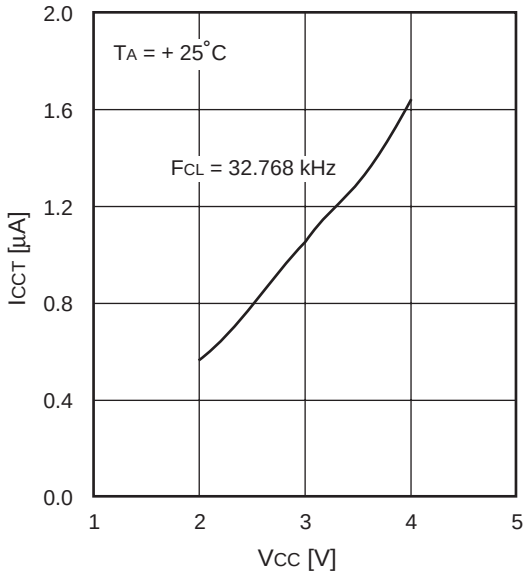
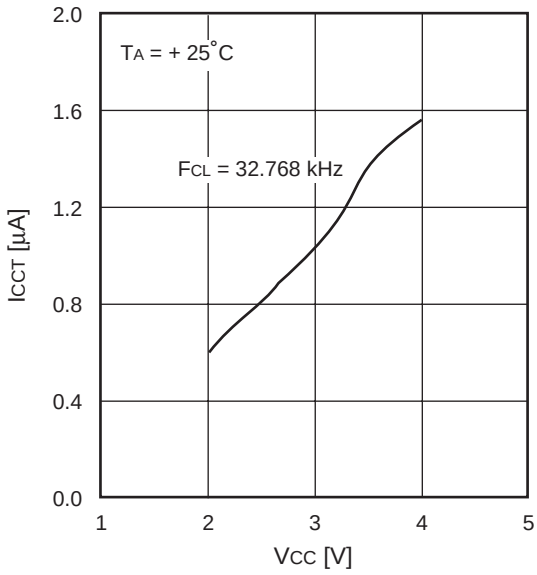
*(Continued)*

ICCT vs VCC (MB89498)

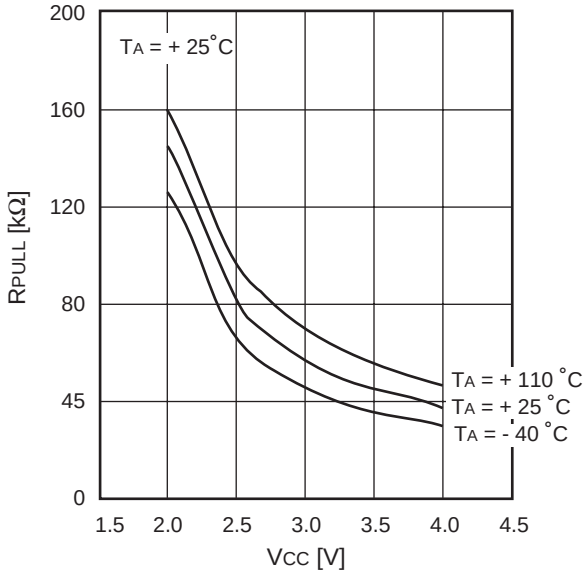



ICCT vs VCC (MB89F499)

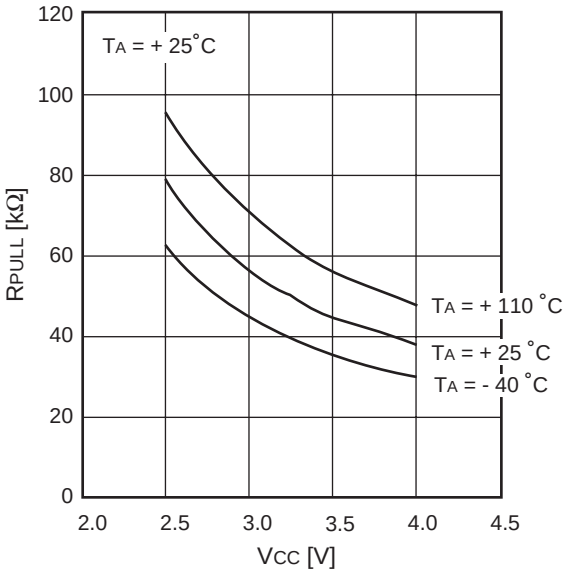



**(4) Pull-up resistance**

RPULL vs VCC (MB89498)




RPULL vs VCC (MB89F499)



## ■ MASK OPTIONS

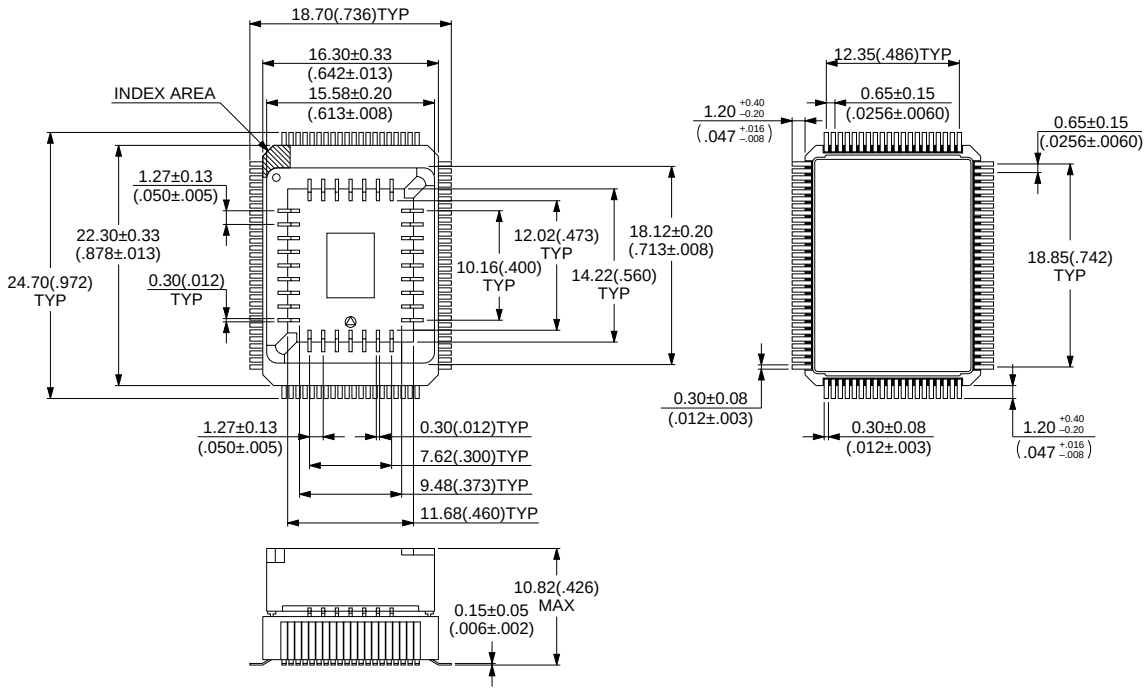
| Part number | MB89498 | MB89F499 | MB89PV490 |
|---|---|---|---|
| **Specifying procedure** | **Specify when ordering mask** | **Setting not possible** | |
| Main clock oscillation stabilizationtime selection<br>$2^{10}/F_{CH}$<br>$2^{14}/F_{CH}$<br>$2^{18}/F_{CH}$ | Selectable | Fixed to oscillation stabilization wait time of $2^{18}/F_{CH}$ | |

## ■ ORDERING INFORMATION

| Part number | Package | Remarks |
|---|---|---|
| MB89498PF<br>MB89F499PF | 100-pin Plastic QFP<br>(FPT-100P-M06) | |
| MB89498PFV<br>MB89F499PFV | 100-pin Plastic LQFP<br>(FPT-100P-M05) | |
| MB89PV490CF | 100-pin Ceramic MQFP<br>(MQP-100C-P01) | |

## ■ PACKAGE DIMENSIONS

100-pin Ceramic MQFP
(MQP-100C-P01)

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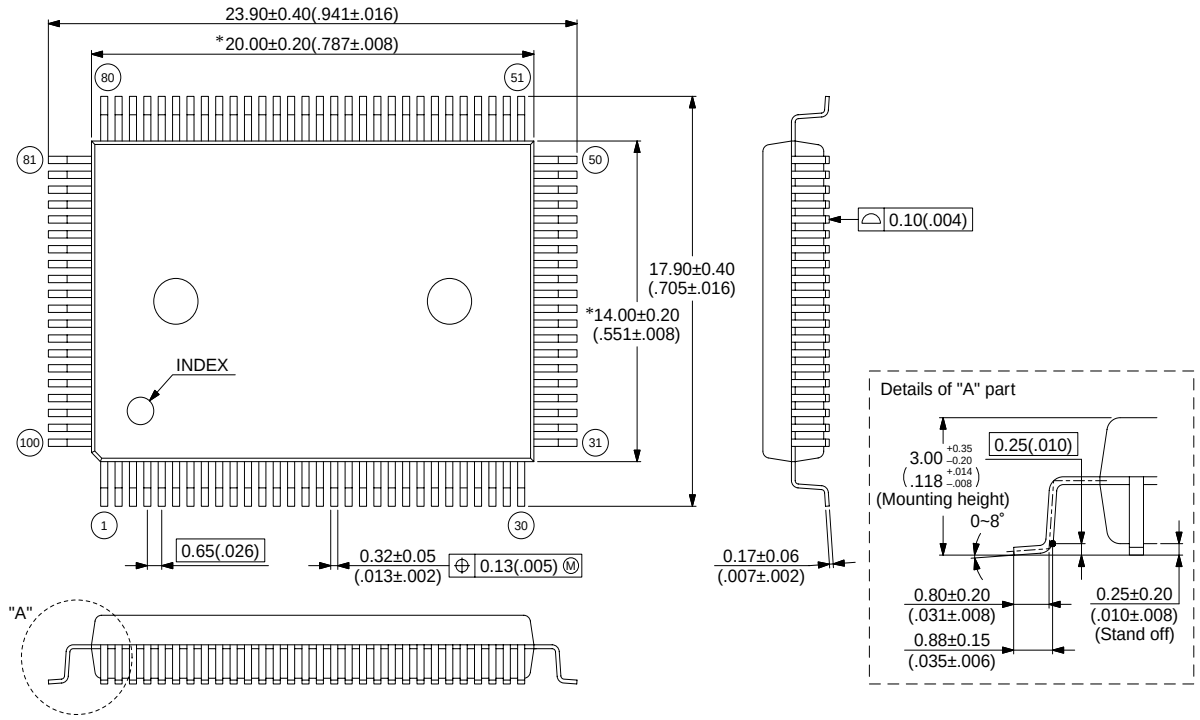
Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

*(Continued)*

100-pin Plastic QFP
(FPT-100P-M06)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

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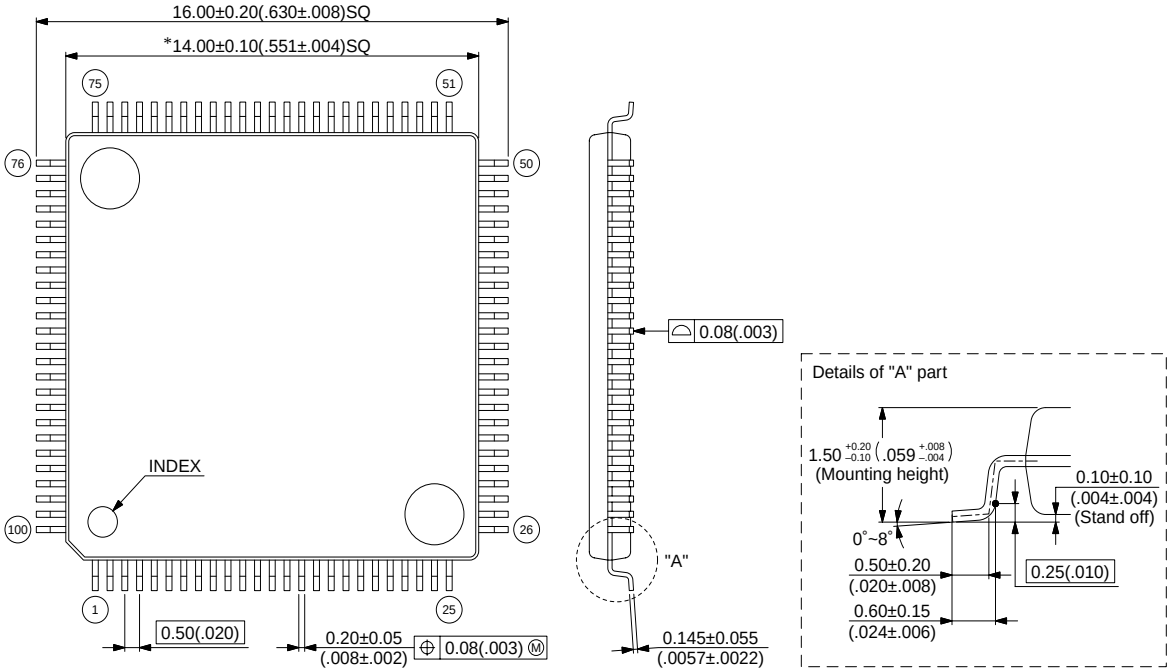
Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

*(Continued)*

*(Continued)*

100-pin Plastic LQFP
(FPT-100P-M05)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.

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Dimensions in mm (inches) .
Note : The values in parentheses are reference values.

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